A Capacitor Bank Simulation Model

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***Abstract*—Power system capacitor banks form critical components of reactive power support and filtering arrangements in high voltage direct current converter stations, such as those connecting electrical power networks with interconnectors, and with offshore wind resources which promise abundant renewable energy but are necessarily distant from centres of demand. Capacitor banks are typically configured in balanced arrangements, where standards require each unit to be measured individually at commissioning and positioned to best balance a neutral or bridge. Capacitor bank rack voltages are tiered but are shared among all units on each rack, which can test dielectrics: this paper presents simulation models to explore distributions of dielectric stress which can result from such arrangements. On a symmetrical rack configured with series-connected units, preliminary results suggest voltages (and therefore electric field stresses) are not evenly shared throughout units in the bank, as: each unit has its own uneven voltage distribution; and rack voltages common to all supported units subject those furthest from a rack tie connection to greater stress than those positioned centrally. Where dielectrics throughout a bank are similar, disproportionate stresses suggest incipient faults and eventual insulation breakdown are more probable for certain unit positions, such as corner units and those at higher voltage. An improved understanding of how unit position affects failure probability could help detect faults, corroborate failure locations detected with reactance techniques, or otherwise direct initial searches for degraded units.**

***Index Terms*—Capacitor, Dielectrics, High Voltage, Simulation**

I. Introduction

Electrical power systems are growing in complexity: a need to replace conventional centrally-located generation with renewables over wide geographies incentivises power factor correction on transmission systems; renewables' intermittency further demands harnessing either energy storage or network diversity; which in turn mean an increasing use of power electronic interfaces (in the form of FACTS devices, to connect generation, and to transfer power over significant distances with HVDC) risks giving rise to harmonics if left unattenuated.

In filtering arrangements (Figure 1), capacitor banks attenuate characteristic harmonics which arise from power-electronic converter interfaces. Such assets are susceptible to 'cascading' degradation [1] and comprise many individual units, making them difficult to maintain. Knowledge of fault locations could thereby: aid maintenance; permit cascading fault interventions; and inform future designs. To these ends, this paper extends investigations on influence of housing on foil voltages in one unit [2] by exploring effects for multiple connected units, and where parallel strings of units share a common rack. It offers an illustrative background to high voltage capacitor banks in Section II before introducing a capacitor rack modelled in COMSOL Multiphysics™. Section III includes results of two studies: voltage distributed over foils of two series-connected units; and a study of an eight-unit rack, which are discussed in Section IV before tentative conclusions are drawn in Section V.

Fig. 1. An HVDC converter station filter hall

II. Background

A selection of capacitor bank arrangements are possible [3]. In an H-bridge configuration, a current transformer connects parallel sides of a bank at a midpoint: sufficient imbalance trips a protection relay which must discern fault conditions from inherent tolerances, failure of redundant elements, and environmental factors such as changing ambient temperature or sunlight heating one side more [4]. For double-Y arrangements, a relay instead measures a neutral connection [5], [6].

Combinations of element size, and parallel and series connections between them can be chosen to achieve desired nameplate ratings; unit sizes designed to balance asset footprint with heat dissipation; and fusing options selected to trade tolerance to dielectric breakdown with operational efficiency [7], where:

1) externally fused banks remove each whole unit from service in the event of failure, and improve visibility;
2) fuseless units short-circuit each faulted series section, reducing reactance (and are the subject of this paper);
3) internally fused designs isolate only failed elements, increasing reactance following each element failure; and
4) metallised-oxide designs offer fault resilience and graceful degradation, but at reduced operational efficiency [8].

TABLE I
SIMULATED MATERIALS

	Al	Steel	Mineral oil	Porcelain
Component	Foils	Housing	Dielectric	Bushings
Conductivity (Sm^{-1})	$30.30e^{6}$	$4.032e^{6}$	$10e^{-15}$	$1e^{-15}$
Relative Permittivity	1	1	4	6

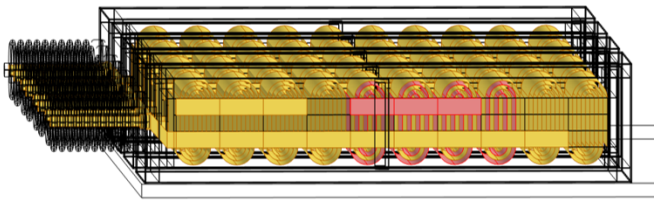

Fig. 2. Foils in a capacitor unit with 5 series groups of 2 elements each

The more evenly capacitor elements are matched, the more evenly are stresses on dielectric shared, and as increased voltage stresses accelerate dielectric aging [1], consequently the less likely any single element is to experience disproportionate stresses such that it would be at risk of premature failure. Accelerated aging further predisposes a bank to cascading element failure: where a failure occurs, dielectrics in the fewer remaining elements (whether those in series with a failed series section in fuseless designs, or those in parallel with a failed element in internally fused designs [4]) are subjected to greater voltages; and effects on asset reactance can moreover expose a weakened bank to greater voltages in practical settings.

Without visible external fuses, large numbers of capacitor units in a bank connected to transmission voltages pose a challenge to early intervention; state of the art detection techniques can locate element failure to one arm of a bridge arrangement [5], significantly reducing uncertainty over fault location for large banks, but still presenting engineers with an unwieldy array of units harbouring a fault. Asset reactance allows faults to be detected, counted, and even located to one of each of four bridge arms on capacitor bank [5], [6], [9], [10].

To connect line voltages within a limited footprint, racks increase in both height and voltage. Rack mounts allow units to adopt different mounting arrangements on a rack, and act as a conduit for voltage to secure unit housings at the potential of a rack tie. Where parallel 'strings' of series-connected units support a common phase, rack faults pose a particular risk where discrepancies exist on a bank and are hard to detect [9].

Figure 2 shows a simplistic design for a set of 4 adjacent units: each comprising 10 discrete-foil elements of 4 turns of aluminium foil, paired to form 5 series element groups amid a relative permittivity $\epsilon_r = 4$ mineral oil dielectric. It reveals foil turns, a draw lead, and a terminal shared by adjacent element groups (in red) for one side of a rack of 8 units in Figure 3. The units modelled omit fuses and use materials in Table I. Figure 3 also illustrates series jumper connections between units on each side (A and B), which connect in parallel to a 40 kV source voltage with a rack tie on Side A.

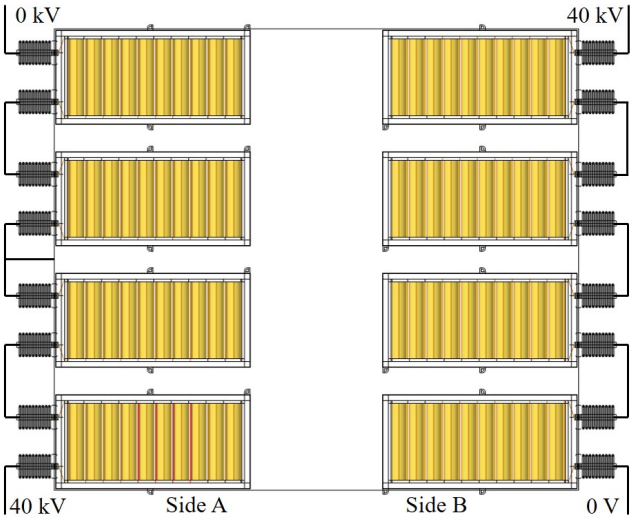

Fig. 3. Foils in a capacitor rack of 8 units

TABLE II
FOIL VOLTAGES ON RACK (KV)

	A1	A2	A3	A4	B1	B2	B3	B4
0	0.000	6.801	11.91	22.13	0.000	5.593	15.67	27.41
1	0.683	8.482	12.83	25.35	0.489	7.385	17.93	29.86
2	1.878	9.982	14.47	28.83	1.379	9.329	20.26	32.37
3	3.385	11.18	16.63	32.46	2.560	11.37	22.62	34.89
4	5.071	11.87	19.22	36.19	3.981	13.49	25.00	37.43
5	6.801	11.91	22.13	40.00	5.593	15.67	27.41	40.00

III. SIMULATION AND RESULTS

Two studies are undertaken: firstly, a single pair of units is modelled in series with a 22 kV source voltage to represent two units between the rack tie and voltage source on Side A; before a study of the complete rack in Figure 3 is conducted.

Connections between units are respectively shown for each study in Figure 4 and in Figure 3, where an electrical circuit interface in COMSOL Multiphysics™ connects: in the first study, unit housings to ground, and both units in series; and for the second, units on each side ('A' and 'B') in series, both sides in parallel to share a common ground, voltage source and an associated resistance, measurement nodes, and a rack tie connection from a jumper between Side A's central units which secures all unit housings on the rack at a shared potential.

Dielectric stress can be approximated with ΔV where $\Delta V_i = V_i - V_{i-1}$ for $V_{-1} = 0$ and for $0 \leq i \leq n, i \in \mathbb{Z}$, the set of n foils. This 'rate of change' in voltage serves to illustrate regions of electric stress placed on dielectrics.

The first study mimics one quarter of a rack. A resulting cut-plane voltage distribution is shown in Figure 4, with results provided in Figure 5, both showing relative change in voltage (ΔV) as a means to approximate dielectric stress.

Secondly, a rack of 8 individual units (Figure 3) is studied with the same interfaces to provide results outlined in Table II and illustrated in Figure 6 and Figure 7.

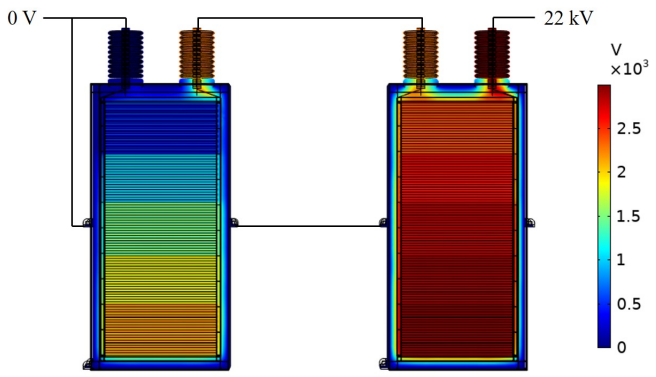

Fig. 4. Voltage shared by units connected to a rack (left) and to 22 kV (right)

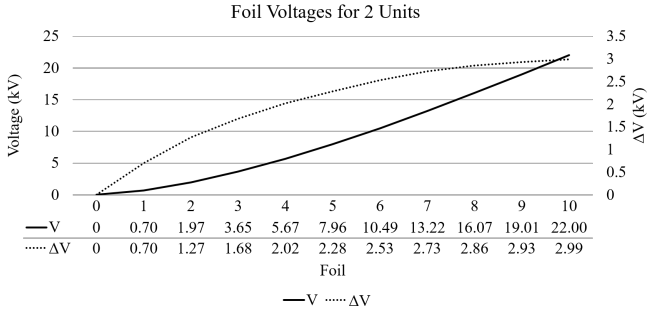

Fig. 5. Voltages shared by adjacent units

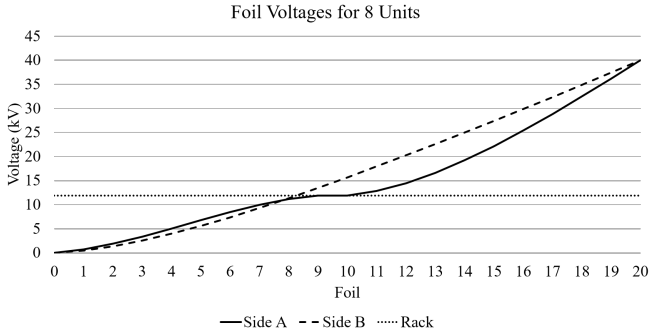

Fig. 6. Foil voltages

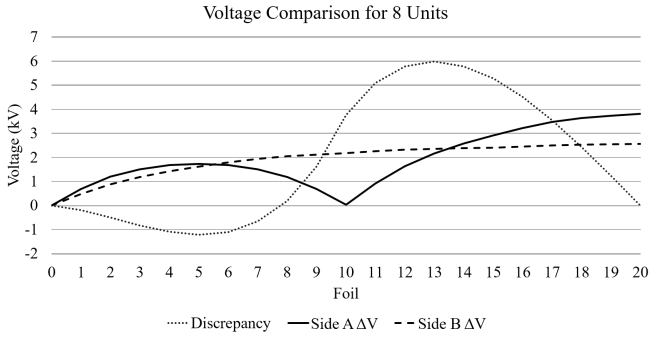

Fig. 7. Foil voltages relative to rack potential

IV. Discussion

A. First Study

Colour variation evident in Figure 4 at a glance reveals an uneven share of stresses, and corresponds with the dotted line in Figure 5. These dielectric stresses result from the relative increase in voltage from one foil to the next, suggesting that the unit connected to voltage is more likely to suffer series element failure, or failure of dielectric between foils and unit housing, than is the case for the unit on the left to which rack voltage is tied. Thus, failures are more likely on units furthest from a rack tie, so numbers of capacitor units on each rack are limited by such disparities between voltages on unit foils and housing, considering strengths of dielectric materials used.

B. Nonlinear Voltage

Figure 5 shows that nonlinear voltage distributions exist beyond any single unit and are present across all series-connected units. In the case of the first study, where there are no complicating factors, this nonlinearity is straightforward.

With a more detailed approach to modelling and therefore larger foil-to-foil capacitances, nonlinearities due to unit housing are found to be less pronounced with more foil turns. This outcome tempers previous findings [2] and serves to highlight the importance of including detail in simulation models.

C. Second Study

For the model in Figure 3 with results in Figure 6, a similar nonlinear distribution is evident in the broken line representing foils on Side B, where there is no rack tie. However, Figure 6 also shows Side A to have an inflection point such that its slopes are steeper and dielectrics consequently more stressed, hence more susceptible to series element failure than Side B.

Rack voltage (the dotted line) reaches only around 30% of the applied voltage as a consequence of this nonlinearity. Differences between voltages on each foil and that of the rack (and unit housings) tests dielectrics most severely in corner units, and particularly those to which connect to high voltage.

D. Effects of a Rack Tie

As only one side ordinarily supports rack voltage, discrepancies inevitably arise. Figure 7 highlights ΔV for each Side A and B, in which the rack tie is shown to influence Side A's ΔV as a local minimum at foil node 10 corresponding with the point of inflection in Figure 6, whereas a broken line representing ΔV for Side B shows only that ΔV increases toward the high voltage connection, and does not match that on Side A. The side supporting rack voltage sees greater stress.

Foil nodes $\{0, 5, 10, 15, 20\}$ represent jumper connections, so the local maximum in ΔV for Side A on foil node 5 occurs where a jumper connects units A1 and A2. Further work would be required (using more comprehensive models) to make certain, but this could suggest such connections to be sites of heightened stress throughout a bank, where midpoints between rack ties - jumpers which connect between racks (or rather, the dielectrics immediately adjacent to these connections) - are likely to experience heightened propensity for stress.

Figure 7 shows a voltage discrepancy ($\Delta V'$) between equivalent foils on each parallel side as a dotted line, where: $\Delta V_i' = V_{i,\ Side\ B} - V_{i,\ Side\ A}$ for i as defined in Section III. Such a discrepancy might be of limited interest for the design considered in Figure 3, but implies a heightened risk of rack faults in capacitor bank designs where separate strings of units have proximal jumper connections. For instance, should distinct unit strings share the same face of a bank, jumper connections between racks would interleave between inner and outer units (as illustrated in [1]), such that this discrepancy due to rack tie distribution could predispose a bank to rack faults.

Manufacturers might prefer to alternate sides which support rack potential, as this could help balance voltage distributions, a bridge or neutral, and additionally aid fault finding in future.

E. Unit Design

All units modelled have draw leads (Figure 2) in a common configuration, but which can be avoided in practical designs by using even numbers of series groups. Where draw leads *are* used, Figure 7 reveals the most stressed terminals on each unit not always to be those at higher voltage, suggesting units are best positioned cognisant of voltage and dielectric stress distributions, with draw leads on the terminal electrically closest to the nearest rack tie, as well as with heat in mind [1]. While voltages age dielectrics, failures ultimately result from electrical field stresses too: bushing connections are a particular risk for field stress, for instance; so units can be designed cognisant of such influences to improve their resilience [11].

F. Cascading Failure

Where one string of capacitor units on a bank determines rack voltages, it follows that a series element failure on the opposing side alters its voltage distribution, so can accentuate the disparity between parallel unit strings. This suggests that not only can series element failure predispose a bank to further breakdown primarily as a result of there being fewer remaining elements and with changed characteristics (such as increased reactance drawing greater voltage), but also that discrepancies between strings are aggravated, heightening risk of rack fault. Were it possible to measure, changes in rack voltages over a bank's operational life might be one means of determining the extent of failures, but only for the supporting string of units.

G. Use of COMSOL

In coupling electrical circuit and electric current interfaces, solution spaces are sensitive: an ability to find a solution depends on the source voltage (V_{sc}), a value of source resistance (R) connected between the source and parallel sides of the capacitor rack, relative permittivity for the dielectric (ϵ_r), and solver error tolerance. For large models, it can take an unpredictable amount of time to reach a solution for a given problem. For the same geometry, mesh, selections, materials, and solver (with relative error 0.005), solutions are found to be at (V_{sc}, R, ϵ_r) = (40 kV, 1 $k\Omega$, 4), and (22 kV, 0.22 Ω, 4).

H. Further Work

1) Layered Materials: COMSOL™ 5.5 supports layered materials, which could be an efficient way to model capacitor windings in future, in terms of: ease of model configuration; enhanced detail; and possibly more efficient computation. This approach would define foils and dielectric layers between them, to create a layered material for use as coherent domains in the geometry, for improved meshing, and which might furthermore allow both solid and fluid dielectrics to be modelled.

2) Larger Models: Work remains to quantify voltage distributions for more detailed simulation models, and to explore the relationship between element failures on one side of a bridge arrangement and subsequent increased stresses on the other due to tiered rack voltages that are common to both sides.

Moreover, stresses are found to be greatest on corner units of a bank, but where it is assumed that voltages distributed on racks themselves are similar in a healthy case: it might instead be the case that some rack levels experience greater overall voltages. Should it be practical to improve simulation efficiency or employ greater computational resources, more of a bank structure can be modelled in detail in future work.

V. Conclusions

Two studies presented in this paper highlight heightened stresses on dielectrics in capacitor units on the edge of a rack, due to nonlinear voltage distributions which extend throughout series connected units in addition to greater potential differences between internal foils and a common rack voltage shared by parallel capacitor unit strings. This has implications for asset design and an understanding of likely failure locations.

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