Potential of Low-Voltage Organic Transistors with High On-State Drain Current for Temperature Sensor Development

Amayikai A. Ishaku and Helena Gleskova *

Department of Electronic and Electrical Engineering, University of Strathclyde, 204 George Street, Glasgow, G1 1XW, United Kingdom

Abstract

Organic transistors with high on-state drain current at gate and drain voltages of −2 V fabricated on polyethylene naphthalate foils were investigated for sensor development. Two aspects were studied: (a) the ability of such transistors to raise the sensitivity of a temperature sensor and (b) the bias stress stability of the transistors subjected to square voltage pulses that turned them on and off repeatedly. To demonstrate the first aspect, the voltage-amplifying ability of the organic transistor was used to increase the response to the temperature, ordinarily achieved with a thermistor. To achieve voltage amplification, the transistor must have on-state drain current of at least 20 μA at gate and drain voltages of −2 V. Two transistors with on-state drain current of ~60 and ~120 μA were tested, leading to voltage gain of −2.8 and −4.9 V/V, respectively, thus increasing the sensitivity of the temperature sensor by a factor of up to 5. To study the second aspect, the same square voltage pulses were concurrently applied to the gate and drain electrodes, causing the transistor to turn on and off repeatedly. The turn-on and turn-off voltages were −2 and 0 V respectively and four different pulse periods were used: *T* of 5, 20, 40 and 60 s. For each *T*, 1000 pulses with turn-on time of 1 s and varying turn-off times were applied to the transistors, leading to the aggregate net stress time of 1000 s in all cases. The changes in the on-state drain

current, threshold voltage, and field-effect mobility depended on T, in spite of the net stress time being the same. The reduction in the on-state drain current did not exceed 17%, stabilization was also observed after about 500 cycles in some cases, and the maximum drop occurred for medium T, thus making $T = 60$ s a favorable condition for sensor operation.

*Contact author: helena.gleskova@strath.ac.uk

Keywords: Organic Field-Effect Transistors, Alkyl Phosphonic Acids, DNTT, Bias Stress, Temperature sensors

1. Introduction

Electronics that offers attributes such as compatibility with plastic and even fabric substrates, low-temperature and large-area fabrication, material application via printing, and adaptability to new form factors is becoming an enabler for wearable applications and robotic skin.[1-4] While most inorganic state-of-the-art devices have limited flexibility and biocompatibility, the adaptation of organic devices in fitness and healthcare applications is growing. [5,6] Organic devices have been shown to provide bio-sensing solutions and can be used in real-time point-of-care environments. [7]

The maturity level of organic transistors based on several conjugated organic materials has spurred sensor development.[8-10] So far much attention has focused on sensing of touch, pressure or force for robotic applications and health monitoring. [10-13] The temperature monitoring using organic electronics is somewhat lagging, although several approaches were reported recently. These include formation of organic diodes [8], operation of the organic transistors in the subthreshold regime [14], and development of temperature-sensitive transistors [15].

Successful implementation of organic transistors in sensors demands their stable operation. It is well established that thin-film transistors based on various material systems suffer from bias stress effect, i.e. their performance changes when voltages are applied. These changes result from gate-source bias that leads to charge trapping in the organic semiconductor, gate dielectric, or at the gate dielectric/semiconductor interface.[16] A stretched-exponential function is often used to describe the kinetics of these changes [17] among which a time-dependent shift of the threshold voltage is dominant [18].

It has been documented that transistors based on well-organized single crystal organic semiconductors do not exhibit any measurable shift in the threshold voltage in the absence of

oxygen and moisture [19], but OTFTs with thin-film organic semiconductors do. The choice of gate dielectric also plays a role and transistors with non-polar and/or hydrophobic dielectrics are more stable. [20] Recently, two new approaches toward more stable transistors have been proposed. They involve the use of CYTOP^{TM} with aluminum oxide/hafnium oxide multilayers that serve as a gate dielectric and a 'barrier' to protect the channel [21] and the incorporation of molecular additives to displace water in polymer transistors [22].

Bias stress experiments with p-channel, low-voltage transistors confirmed that application of a more negative gate-source voltage leads to faster threshold voltage shift, while application of a more negative drain-source voltage leads to slower threshold voltage shift [23], i.e. the transistors exhibit slower degradation when operating in the saturation regime. The increased drain-source electric field leads to a decrease in total hole concentration in the channel and is thought to help with the release of the trapped charges into the mobile states, both slowing the rate of the transistor degradation.[18]

OTFT bias stress experiments tend to be performed with constant (DC) voltages and the application of alternating voltages (AC) is underreported. AC bias stress was reported for poly(quarterthiophene) organic transistors using square pulses with repetition time of up to 100 ms and varied duty cycle.[24] The authors observed that the transistor recovery exhibited short- (charge carriers trapped in shallow traps) and long-lived (charge carriers trapped in deep traps) components. Consequently, a deliberate pausing of the transistor bias may provide recovery time for the transistor. Forcing the transistor to alternate between the on- and off-states would be suitable for flexible sensors that do not demand frequent data collection, i.e. the sensor/transistor can be turned off when the data is not collected.

Organic transistors that combine low-voltage operation with high on-state drain current would be able to amplify any changes occurring in their gate voltage as a result of physical stimulus. Such transistors, when fabricated on plastic substrates, can benefit flexible sensor development, as they would replace rigid silicon transistors. Organic thin-film transistors based on dinaphtho[2,3-b:2′,3′-*f*]thieno[3,2-*b*]thiophene and ultra-thin gate dielectric composed of aluminum oxide functionalized with a monolayer of alkyl phosphonic acid (gate dielectric capacitance of ~ 0.5 μF/cm^2) have shown low-voltage operation, high on-state drain current, and low bias stress effect. [18,25-27] This paper explores application of such transistors fabricated on polyethylene naphthalate (PEN) foil for sensor development. The first part shows how such a transistor amplifies any changes occurring in its gate voltage as a result of physical stimulus. While the chosen physical stimulus is changing temperature, the presented results demonstrate the potential and the guiding principles for the future sensor development. In the second part we addresses the bias stress stability. Contrary to any prior work, we studied the effect of long voltage pulses and low repetition rates that intentionally induce the recurring turn-on/turn-off of a transistor and are applicable to flexible sensors that do not demand frequent data collection, i.e. the sensor/transistor can be turned off when the data is not collected.

2. Experimental procedures

Low-voltage bottom-gate, top-contact p-type organic thin-film transistors (OTFTs) based on dinaphtho[2,3-b:2′,3′-*f*]thieno[3,2-*b*]thiophene (DNTT) were fabricated according to the procedure described in Reference 24 on PEN (Optfine PQA1, DuPont Teijin). The low-voltage operation was achieved by using a thin, bi-layer gate dielectric consisting of aluminum oxide (AlO_x) prepared by UV/ozone oxidation [28] and an octadecyl phosphonic acid ($C_{18}PA$) (Strem

Chemicals) monolayer prepared in vacuum [27]. The cross-section of the transistor is shown in Fig. 1(c).

The fabrication procedure was as follows. A 30-nm-thick aluminum layer was evaporated on the substrate at a rate of ~ 2 Å/s. Part of the gate electrode was coated with a 40-nm-thick Au to prevent its oxidation. Next, AlO_x was prepared by exposing the aluminum to UV/ozone (UVOCS, USA) in ambient atmosphere for 60 minutes. To prevent the contamination of the oxidizing surface, the UV/ozone cleaner was enclosed under a Hepa filter. AlO_x preparation by UV/ozone oxidation of thermally evaporated aluminum has been reported elsewhere [29]. Approximately 20 nm of $C_{18}PA$ was deposited in Mini-SPECTROS (K. J. Lesker, U.K.) evaporation chamber enclosed in a N_2-filled glove box (Jacomex, France). The evaporation rate was about 3 Å/s and the substrate was kept at room temperature. Afterwards, the substrate temperature was raised to ~ 160°C for 3 hours to remove all physisorbed molecules and to form a monolayer. The resulting capacitance of this bi-layer dielectric, measured on corresponding metal-insulator-metal structures with areas between 0.1 and 0.4 mm^2, is 0.30±0.029 $\mu F/cm^2$. Next, a 25-nm-thick DNTT layer (Sigma Aldrich, U.K) was thermally evaporated at a rate of 0.5 Å/s at room temperature. Finally, a 80-nm-thick Au layer was evaporated at a rate of ~ 3 Å/s to complete the transistors. Source-drain masks (Ossila, UK) with interdigitated contacts were used, leading to channel length of ~40 μm and channel width of 18.23 mm. The top view of the transistor is shown in Fig. 1(d). The OTFT characteristics were measured with Agilent B1500A semiconductor device analyzer in a sweep mode. To measure the transfer characteristics the gate-to-source voltage V_{GS} was swept from 0 to −2V and back. To measure the output characteristics, the drain-to-source voltage V_{DS} was swept from 0 to −2V and back. An example of the transfer and output characteristics is shown in Fig. 1(a) and 1(b) respectively.

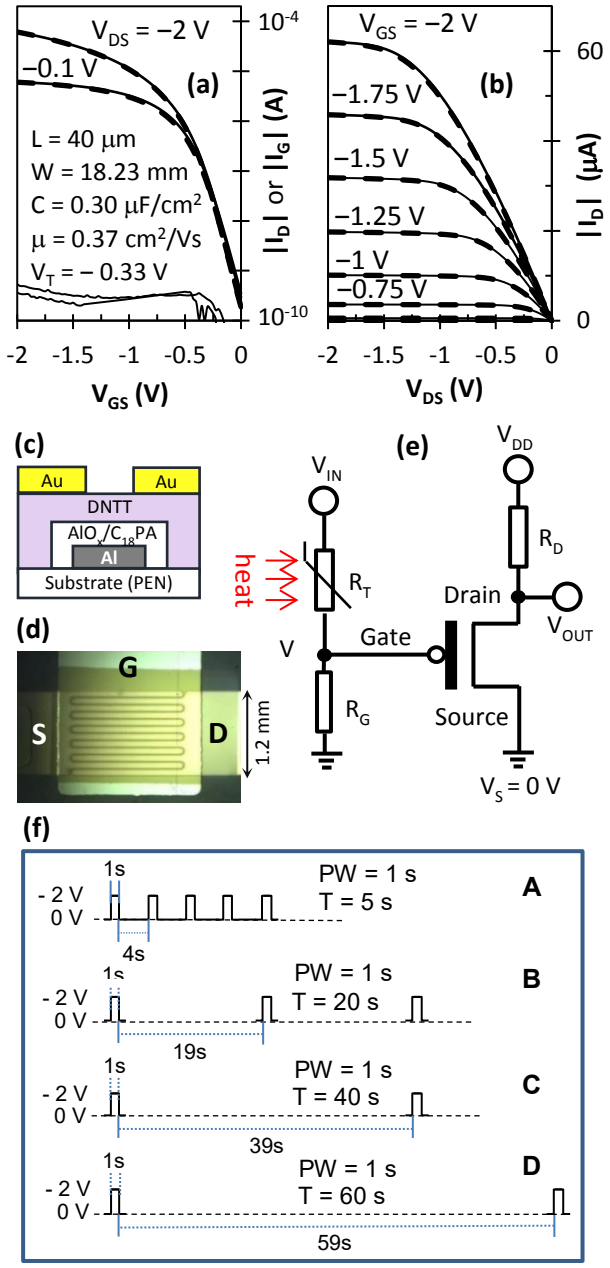


Figure 1. OTFT transfer (a) and output (b) characteristics; OTFT cross-section (c); top view of the transistor (d); schematic of the temperature sensor (e); and bias stress voltage pulse signals (f) with pulse width *PW* of 1 s, on-state and off-state voltages of −2 and 0 V, and period *T* of 5 s (A), 20 s (B), 40 s (C) and 60 s (D). The solid lines in (a) and (b) correspond to voltage sweep from 0 to –2 V and the dashed lines to sweep from –2 to 0 V.

A commercially-available thermistor with negative temperature coefficient and nominal resistance of 100 kΩ (Farnell, NTCLE100E3104J) was selected to respond to the changes in temperature, while the OTFT provided the desired amplification. To simplify the mathematical analysis of the sensor response only the thermistor was heated during the sensor measurements. To assemble the sensor of Figure 1(e), the resistors and the thermistor were soldered onto a stripboard and connected to OTFT via gold wires, attached to the transistor terminals using silver paste. The thermistor had extended leads to allow its placement on a Peltier element controlled via LabVIEW. To provide optimum heat transfer, the thermistor was 'embedded' in thermally conductive paste. The operation of the sensor was analyzed by applying a range of voltages V_{DD} and monitoring the voltages on the gate and drain of the transistor.

During the bias stress of the transistor, the same square pulses, consisting of a high-value of −2 V (to turn the transistor on) and low-value of 0 V (to turn the transistor off), were applied to the gate and drain electrodes, while the source was grounded. Consequently, when the transistor was turned on, it operated in the saturation regime. The turn-on time was kept at 1 s, while the turn-off time was varied from 4 s to 59 s, leading to a pulse period T ranging from 5 to 60 s. Different transistors were subjected to different bias stress pulses shown in Fig. 1(f). In addition, one transistor was subjected to a DC bias stress with $V_{GS} = V_{DS} = -2$ V and the source grounded. Each transistor was subjected to 1000 pulses or a DC bias stress of 1000 s, i.e. the net bias stress time was 1000 s for each OTFT, while the actual measurement time varied from ~17 minutes to ~17 hours. The transfer characteristic of each transistor was measured before the bias stress and the transistor drain current was monitored during the bias stress. The bias stress was quickly interrupted after every 100 pulses and the transistor transfer characteristic was measured for $V_{DS} = -2$ V. This allowed additional monitoring of the threshold voltage V_T, field-effect

mobility μ, and subthreshold slope S. The mobility and the threshold voltage were extracted by using the steepest section of the $I_D^{1/2}$ versus V_{GS} data.

3. OTFT temperature sensor

3.1. Results

Fig. 2(a) shows a response of the thermistor in the temperature range from 20 to 50°C. The resistance R_T of the thermistor decreases with the increasing temperature, leading to R_T = 128 kΩ at 20°C and 34.3 kΩ at 50°C. The organic transistor has high input impedance and the voltage V_{IN} applied on the input of the sensor produces current flowing through R_T and R_G into ground. That sets the voltage V_G on the gate of the transistor as follows:

$$V_G = \frac{V_{IN}}{R_T + R_G} \cdot R \quad (1)$$

Fig. 2(b) shows the effect of resistor R_G on the voltage V_G for V_{IN} = −4 V. Equation (1) was used to calculate V_G. R_G was increased from 10 kΩ to 100 kΩ with increment of 10 kΩ. Taking into account that the transistors have threshold voltage of ~ −0.3 V, the variation of V_G between −1 and −2 V would be optimal. Let say the aim of the sensor is to measure the body temperature, i.e. the temperature from ~20 to ~40°C. One would conclude from this graph that to meet the above requirements, the suitable value of R is ~50 kΩ. Lower R_G shifts the temperature band to higher temperatures while higher R_G shifts the temperature band to lower temperatures. In addition, the variation of V_G between −1 and −2 V leads to a nearly linear drop in V_G with the rising temperature, leading to a nearly linear response of the sensor output voltage (see Fig. 3(c)).

Two transistors with different on-state drain current were tested in the sensor. Their transfer characteristics for V_{DS} = –0.1 V and –2 V are shown in Figs. 1(a) and 2(c). At V_{DS} = V_{GS} = –2 V the drain current of the transistor of Fig. 1(a) is 61 μA, while the drain current of the transistor of Fig. 2(c) is 126 μA (L is reduced to 20 μm in this case).

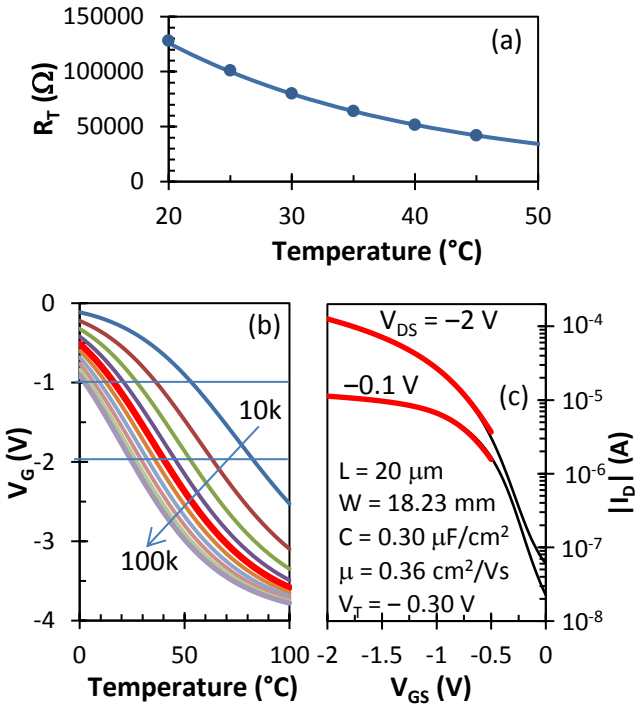


Figure 2. Thermistor resistance as a function of the applied temperature (a); V_G as a function of temperature applied to the thermistor calculated using Eq. (1) with R_G as a parameter (b); and transfer characteristics of OTFT used for mathematical verification of the sensor model (c). The thick red line in (b) is for R_G = 50 kΩ. The red lines in (c) represent the transistor model (see below) implemented into the sensor model.

Table 1 compares the values of V_G obtained in 3 different ways: (a) calculated using Eq. (1), (b) measured for V_{IN} = −4 V and R_G = 50 kΩ when the transistor is disconnected, and (c) measured on the gate of the transistor in the fully assembled sensor with V_{IN} = V_{DD} = −4 V, R_G = 50 kΩ, and R_D = 47 kΩ. Similar voltages are achieved with or without the transistor being

connected, confirming that the transistor has high input impedance and does not affect the left side of the circuit that contains the thermistor.

Table 1. Voltage V_G on the gate of the transistor; [a] V_G calculated using Eq. (1), [b] V_G measured on the output of the voltage divider (transistor is disconnected), [c] V_G measured on the gate of the transistor in the fully-assembled sensor (R_G = 50 kΩ, R_D = 47 kΩ, V_{IN} = V_{DD} = –4 V).

T (°C)	V_G (V)		
	Eq. (1) [a]	Voltage divider [b]	Full sensor [c]
20	-1.136	-1.133	-1.132
25	-1.333	-1.342	-1.331
30	-1.541	-1.561	-1.548
35	-1.753	-1.778	-1.764
40	-1.966	-1.993	-1.987
45	-2.173	-2.207	-2.194
50	-2.372	-2.411	-2.394

Fig. 3 shows the results of the complete sensor for V_{IN} = −4 V, R_G = 50 kΩ, R_D = 47 kΩ, and the OTFT of Figure 2(c). Fig. 3(a) shows V_G as a function of V_{DD}, Fig. 3(b) shows V_{OUT} as a function of V_{DD}, Fig. 3(c) shows V_{OUT} as a function of temperature applied to the thermistor, and Fig. 3(d) shows repeated measurements of V_{OUT} as a function of V_G for two different OTFTs. As expected, the voltage on the gate of the transistor is not affected by the value of V_{DD}. V_{OUT} increases with rising V_{DD}. For lower values of V_{DD} the output voltage V_{OUT} increases linearly with a slope of about 0.18. This corresponds to the transistor operating in the linear regime. When the supply voltage V_{DD} is high enough to place the transistor into saturation, the slope of V_{OUT} versus V_{DD} becomes ~1. Finally, V_{OUT} decreases with rising temperature regardless of the supply voltage V_{DD}. When the OTFT of Figure 2(c) operates in saturation, the change in V_{OUT} is ~ –200 mV/°C and the decrease is approximately linear.

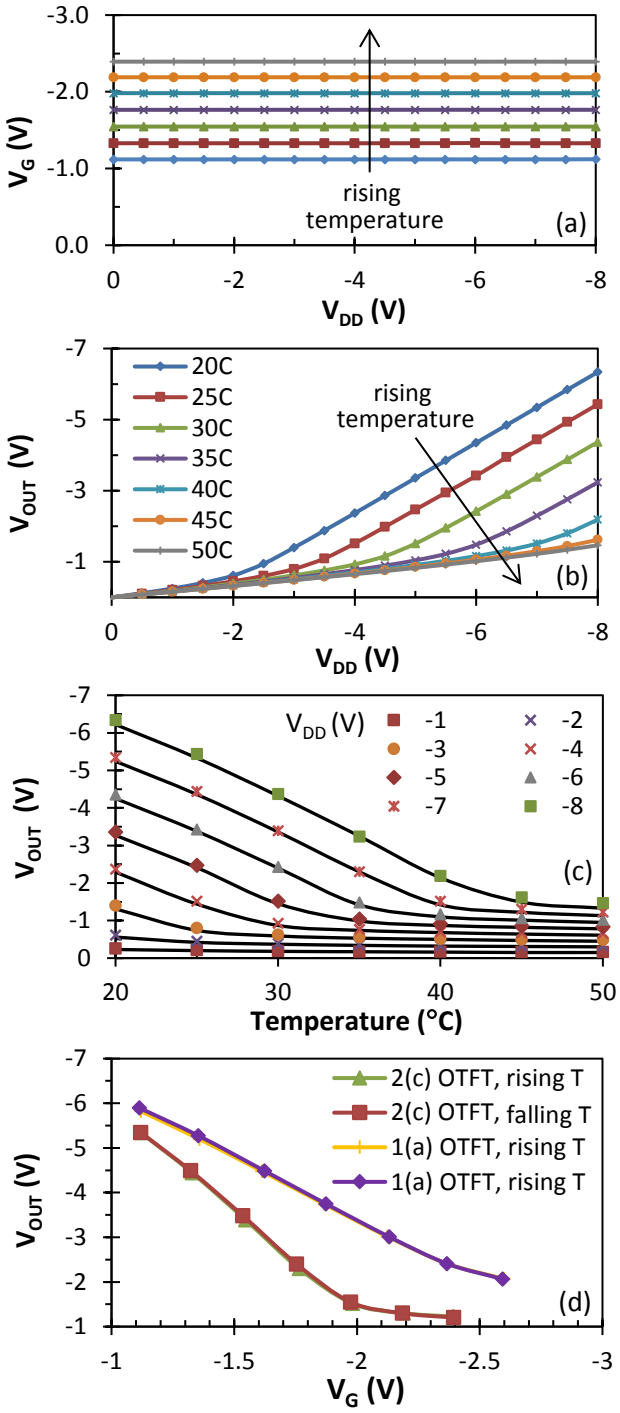


Figure 3. Measurements of the temperature sensor for R_G = 50 kΩ, R_D = 47 kΩ, and V_{IN} = –4 V. V_G as a function of V_{DD} for temperatures from 20 to 50°C (a); V_{OUT} as a function of V_{DD} for OTFT of Fig. 2(c) and temperatures from 20 to 50°C (b); V_{OUT} of (b) as a function of temperature (c); and repeated measurements of V_{OUT} for V_{DD} = –7 V and OTFTs of Figs. 2(c) & 1(a) as a function of V_G (d). The solid lines in (a), (b) and (d) are guides to the eye, while the solid black lines in (c) correspond to the sensor model described below. V_G and V_{OUT} are referenced to V_S/ground.

The response to temperature becomes substantially weaker at higher temperatures when the voltages on the terminals of the transistor force it to work in the linear regime. In such a case V_{OUT} responds to the changing temperature at a rate of ~ –1.3 mV/°C and the decrease is again linear. Consequently, the main aim of the sensor design is to assure that the transistor operates in the saturation regime within the whole range of desired temperatures. Based on the data of Fig. 3(c), this sensor is ideally suited for measuring body or ambient office temperature in the range from 20 to 40°C, if V_{DD} between –7 and –8 V is selected. Finally, Fig. 3(d) shows repeated measurements of V_{OUT} versus V_G for both OTFTs and V_{DD} = –7 V. Both transistors show good repeatability; however, the OTFT with higher on-state drain current exhibits stronger response to the changes in temperature.

3.2. Discussion

The organic transistor of Fig. 2(c) was used in the sensor model. During the operation of the sensor, the transistor transitions between linear and saturation regimes, depending on the relationship between V_G and $V_D = V_{OUT}$. However, the MOSFET equations can only describe the transistor in linear or saturation regimes separately. Consequently, we need a single analytical expression for I_D that will capture the full behavior of the transistor and thus the sensor. We have shown previously [30] that the drain current of the transistor can be modeled as:

$$I_D = \frac{W}{L\left(1-\frac{\Delta L}{L}\right)} \cdot \frac{\mu_o}{\left(\frac{V_{SS}}{2+\gamma}\right)^{\gamma}} \cdot C \cdot \left[\frac{(VS_{EODR})^{(\gamma+2)}}{\gamma+2} - \frac{(VD_{EODR})^{(\gamma+2)}}{\gamma+2}\right] \quad (2)$$

where VS_{EODR} and VD_{EODR} is the effective voltage overdrive on source and drain side of the transistor, respectively. If the source/drain contact resistance is neglected, they are:

$$VS_{EODR} = V_{SS}\ln\left\{1 + \exp\left[\frac{V_G - V_T - V_S - (V_G - V_S)\delta_{VT}}{V_{SS}}\right]\right\} \quad (3)$$

$$VD_{EODR} = V_{SS}\ln\left\{1 + \exp\left[\frac{V_G - V_T - V_{OUT} - (V_G - V_{OUT})\delta_{VT}}{V_{SS}}\right]\right\} \quad (4)$$

$\Delta L/L$ represents the channel length modulation. When the transistor is turned on, which is the case of the temperature sensor, it can be expressed as:

$$\frac{\Delta L}{L} = \lambda(V_{OUT} - V_S) \cdot \frac{(V_{OUT} - V_S) + (V_G - V_T)}{2(V_{OUT} - V_S) + (V_G - V_T)} \geq 0 \quad (5)$$

Here V_G, V_{OUT}, and V_S are voltages on the gate, drain and source terminals respectively. $V_S = 0$ and V_G and V_{OUT} are referenced to V_S. W is the channel width, L the channel length, C the gate dielectric capacitance and V_T the threshold voltage of the transistor. The measured values of W, L, C, and V_T (listed in Fig. 2(c)) were used in the model. Furthermore, the channel modulation factor $\lambda = 0.02$. The remaining parameters, so called 'fitting parameters', are the subthreshold slope V_{SS}, mobility enhancement factor γ, low-field mobility μ_o, and the threshold voltage bias sensitivity δ_{VT}. They are determined by obtaining a least-square fit of Eq. (2) to the data of Fig. 2(c). The result of such fitting is demonstrated by the red lines in Fig. 2(c). The result shows that Eq. (2) reproduces the transistor transfer characteristics well and thus enables calculation of V_{OUT} of the

sensor. The advantage of using Eq. (2) is that the same four fitting parameters reproduce the transistor behavior both in the linear and saturation regime.

The black lines in Fig. 3(c) show the calculated V_{OUT} for the transistor of Fig. 2(c). A very good agreement between the measurement (points) and the calculation (black lines) is achieved. The calculation included Eqs. (1)-(5) plus one additional equation that applies to the right side of the sensor:

$$V_{OUT} = V_{DD} - R_D \cdot I_D \tag{6}$$

In the desired temperature range from 20 to 40°C the gate voltage V_G changes from –1.12 (20°C) to –1.98 V (40°C), i.e. by 0.86 V (see Fig. 3(a)). If this voltage was 'read out' without the addition of the transistor, such sensor would have sensitivity of 43 mV/°C for V_{IN} = −4 V and R_G = 50 kΩ. The addition of the transistor increases that sensitivity by a factor of up to ~ 5.

As can be seen in Fig. 3(d), OTFT of Fig. 2(c) exhibits bigger changes in V_{OUT} than OTFT of Fig. 1(a) and this results from the on-state drain current being about a factor of two higher for the former OTFT. By taking the slope of V_{OUT}/V_{IN} the voltage gain of both transistors can be calculated, leading to the maximum value of −4.94 V/V for the OTFT of Fig. 2(c) and −2.79 V/V for the OTFT of Fig. 1(a). Consequently, the voltage gain of the transistor scales approximately linearly with the OTFT on-state drain current that should exceed ~20 μA at $V_{GS} = V_{DS}$ = −2 V, should the transistor provide amplification of the sensor signal.

Given that Eqs. (1)-(6) accurately model the sensor output, one can use them for future sensor design, e.g. by limiting the voltages V_{IN} and V_{DD} to certain values and selecting R_G and R_D for the maximum sensitivity and linear output. While the effect of these parameters is quite complex, the following guiding principles should be observed: (a) V_{IN} and R_G determine the

OTFT gate voltage V_G. This voltage should be higher than the OTFT threshold voltage but low enough to enable the saturation operation of the transistor without the need for excessive $V_D = V_{OUT}$. V_D is restricted by the breakdown voltage of the OTFT gate dielectric; (b) the transistor bias stress instability has been observed to increase with rising V_G [23] and lower V_G can accomplish stable sensor operation more easily; (c) R_D controls the voltage gain of the transistor, i.e. the sensitivity of the sensor – lower R_D leads to lower voltage gain but requires lower V_{DD} while higher R_D leads to higher gain but requires higher V_{DD}. Ultimately there is a trade-off between the gain and the supply voltage V_{DD}.

Finally, the use of the sensor model presented here can be extended to OTFTs with other geometries, materials, or channel dimensions. Since the optimization and accurate prediction of the sensor output incorporates the measured transfer characteristics of the OTFT selected for the sensor, factors such as source/drain contact resistance, voltage-dependent carrier injection, interface barriers and traps, etc., are embedded into the fitting parameters of Eq. (2) and their knowledge is generally not required. However, if the OTFT source/drain contact resistance cannot be neglected, Eqs. (3) and (4) can be modified to include the contact resistance, as shown in [31].

4. OTFT pulsed bias stress

4.1. Results

Next, a new bias stress protocol that is applicable to sensors with low data rate collection is presented. This protocol assumes that the sensor/transistor can be turned off when the data is not collected. Figure 4 shows the transistor on-state drain current (at $V_{GS} = V_{DS} = -2$ V), threshold voltage, and field-effect mobility as functions of the net bias stress time. The drain

currents and field-effect mobilities are normalized to their pre-bias-stress values, $\frac{I_{ON}(t)}{I_{ON}(0)}$ and $\frac{\mu(t)}{\mu(0)}$, while the threshold voltage shift $\Delta V_T = V_T(t) - V_T(0)$ is used to evaluate the changes in the threshold voltage. Furthermore, the following stretched-exponential functions were fitted to the data:

$$\frac{I_{ON}(t)}{I_{ON}(0)} = \alpha_{I_{ON}} + \left[1 - \alpha_{I_{ON}}\right] e^{-\left(t/\tau_{I_{ON}}\right)^{\beta_{I_{ON}}}} \quad (7)$$

$$\Delta V_T = V_T(t) - V_T(0) = \alpha_{V_T}\left[1 - e^{-\left(t/\tau_{V_T}\right)^{\beta_{V_T}}}\right] \quad (8)$$

$$\frac{\mu(t)}{\mu(0)} = \alpha_{\mu} + \left[1 - \alpha_{\mu}\right] e^{-\left(t/\tau_{\mu}\right)^{\beta_{\mu}}} \quad (9)$$

where $\alpha_{I_{ON}}$, α_{μ} are the steady-state values of normalized drain current and mobility for $t \to \infty$, α_{V_T} is the threshold voltage shift at infinity; $\tau_{I_{ON}}$, τ_{V_T}, τ_{μ} are the time constants and $\beta_{I_{ON}}$, β_{V_T}, and β_{μ} are stretching parameters corresponding to I_{ON} (I_D at $V_{GS} = V_{DS} = -2$ V), V_T and μ. t is the net bias stress time, i.e. the aggregate transistor turn-on time. Stretched-exponential fits were first introduced for transistors based on hydrogenated amorphous silicon to describe the threshold voltage shift induced by the bias stress. While the time constant represented the speed of the degradation process, the stretching parameter reflected the dispersive process of the charge carrier trap creation.

Regardless of the pulse period, the OTFT was turned on for 1 s during each period by simultaneously applying $V_{GS} = V_{DS} = -2$ V. Therefore the increasing T means that the transistor off-time increases. One can also think of the DC bias stress as a 'pulsed' bias stress with zero off-time. Consequently, going from DC to $T = 60$ s, the transistor turn-off time is rising from 0 s to 59 s, while the aggregate turn-on time remains the same. Therefore, the only difference

between the bias stress conditions is the length of time for which the transistor is turned off. The results of Fig. 4 suggest that this off-time plays a significant role.

Fig. 4(a) shows the normalized on-state drain current for different pulses. $\tau_{I_{ON}}$ and $\beta_{I_{ON}}$ obtained using Eq. (7) are also shown. The DC bias stress led to an initial increase in $|I_{ON}|$ of about 1.6%, followed by a decrease of 3.2% from its initial value. Eq. (7) cannot reproduce this initial increase and $\beta_{I_{ON}}$ was set to its maximum value of 1. Going from T = 5 s to 60 s the steady-state values of the normalized on-state drain current for $t \to \infty$ are 0.93, 0.87 and 0.92 and reductions in $\tau_{I_{ON}}$ and $\beta_{I_{ON}}$ are observed. The time constant decreased from 394 to 338 to 202 s and the stretching parameter from 0.74 to 0.60 to 0.45. This indicates that the increasing off-time leads to a more dispersive degradation process with shorter time constant. Yet, the final steady-state values differ from each other by less than 7%. At the same time, please recall that while the DC bias stress corresponds to 1000 s (≈ 17 minutes) of measurement time, the pulsed bias stress with T = 60 s equals to the total measurement time of 60000 s (≈ 17 hours).

Changes in the threshold voltage, field-effect mobility, and the subthreshold slope lead to changes in the on-state drain current and are discussed next. The pre-bias-stress values of the subthreshold slope were ~110 mV/decade and the random variations of up to ±4% during the bias stress are not considered. Fig. 4(b) shows the measured threshold voltage shift $|\Delta V_T|$ as a function of the net bias stress time, for different T. The stretched-exponential fits of Eq. (8) are also shown. The final value of the DC bias stress is shown for comparison as well. The threshold voltage increases in all cases. After 1000 s of net bias stress, the pulses with T = 5 s lead to an increase in $|V_T|$ of about 50 mV (similar to DC bias stress), followed by T = 60 s with $|\Delta V_T|$ of ~ 100 mV, and T = 20 s with $|\Delta V_T|$ of ~ 110 mV. The corresponding steady-state values at $t \to \infty$ are 86, 164 and 144 mV, with increasing T. Both the τ_{V_T} and β_{V_T} decrease with increasing T. τ_{V_T}

decreased from 1140 to 780 to 732 s and β_{V_T} from 0.50 to 0.46 to 0.34. Similar to the case of the on-state drain current, this indicates a more dispersive degradation process with shorter time constant as T increases. Overall, $|\Delta V_T|$ as a function of T appears to stabilize or go through a maximum and longer off-times are not detrimental.

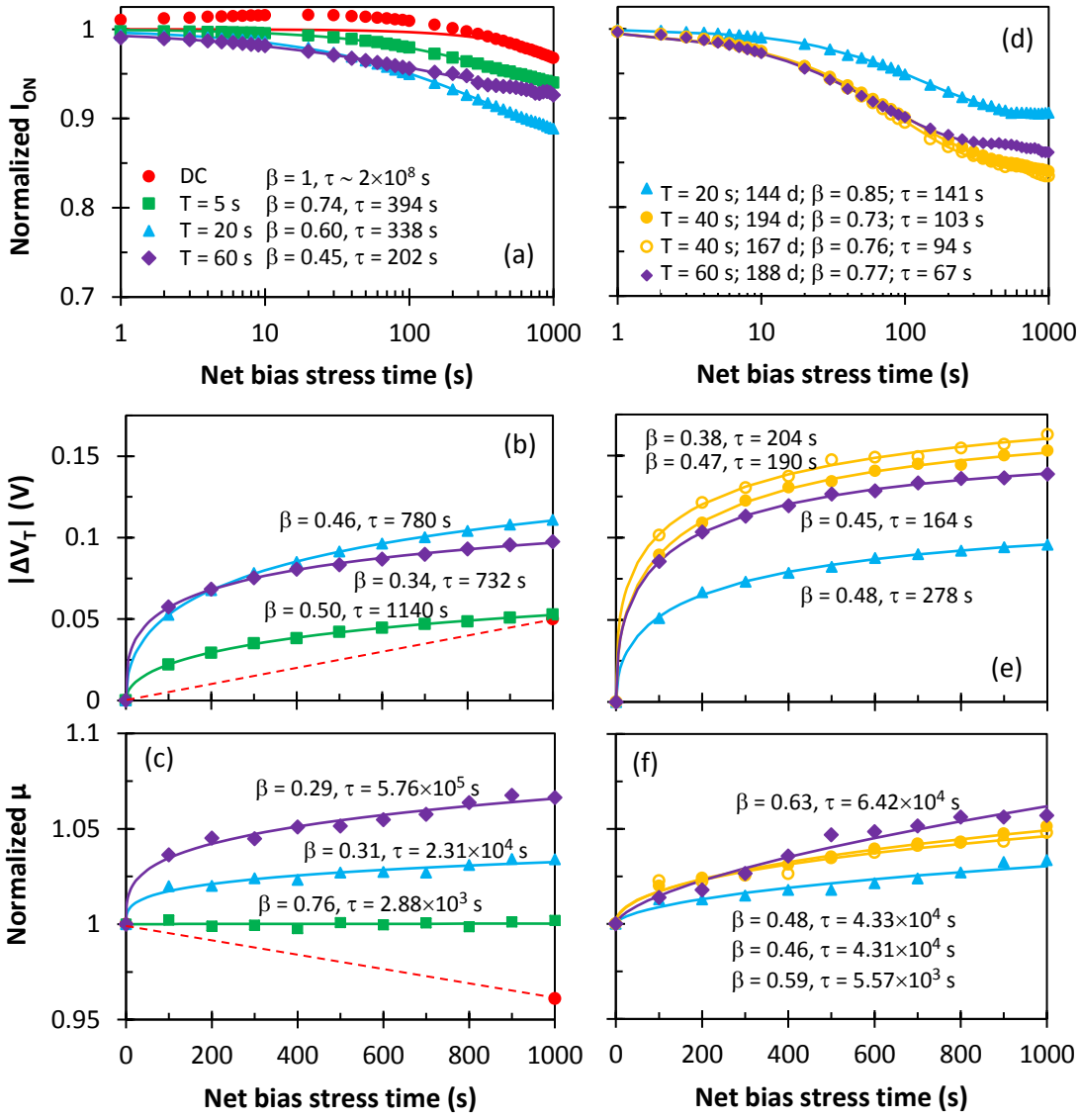


Figure 4. Normalized on-state drain current (a,d), threshold voltage shift (b,e) and normalized field-effect mobility (c,f) as functions of net bias stress time for fresh (a,b,c) and aged (d,e,f) OTFTs. The 'aging' is given in days in (d). Points correspond to the measured data and the lines represent the stretched-exponential fits of Eqs. (7)-(9).

Fig. 4(c) shows the measured normalized field-effect mobility as a function of the net bias stress time and the stretched-exponential fits of Eq. (9). The normalized μ for DC bias stress is also shown for comparison. The field-effect mobility shows almost no change for pulses with T = 5 s. T = 20 s and 60 s show an increase of 3.4% and 6.6%, respectively. For pulsed bias stress the mobility exhibits a rise, while a reduction in the mobility of about 4% is seen for DC bias stress. As T increased from 5 to 60 s, the normalized steady-state value for $t \rightarrow \infty$ increased from 1.00 to 1.10 and 1.46, respectively. At the same time τ_{μ} increased from 2.88 x 10^3 to 5.76 x 10^5 s, while β_{μ} decreased from 0.76 to 0.29. Overall, the longer the off-time the bigger is the increase in the field-effect mobility.

Figs. 4(d)-(f) show the changes in the on-state drain current, threshold voltage, and field-effect mobility for transistors that were 'aged' for 5-6 months in dark ambient air and then measured with pulse periods of 20, 40 and 60 s. Two transistors were bias stressed for T = 40 s to check the reproducibility. The stretched-exponential functions were again fitted to the data; however, the mobility fits should be taken with caution due to the larger scatter in the data. The results show that the degradation of the on-state drain current proceeds faster; yet, there is a sign that the drain current reaches a steady-state value within ~ 500 s. These steady-state values of the normalized on-state drain current are 0.90 for T = 20 s, 0.84 for both measurements at T = 40 s and 0.87 for T = 60 s. These values are up to 6% smaller than those of fresh transistors. In addition, all time constants are reduced and the stretching parameters increased. Fig. 4(e) shows an increase in the threshold voltage for all pulses. Again, T = 60 s shows smaller $|\Delta V_T|$ when compared to T = 40 s. The steady-state values of $|\Delta V_T|$ at $t \rightarrow \infty$ are 114 mV for T = 20 s, 171/191 mV for T = 40 s, and 155 mV for T = 60 s. When compared to data of Fig. 4(b), $|\Delta V_T|$

for T = 20 s is slightly smaller while $|\Delta V_T|$ for T = 60 s is slightly higher. Furthermore, all time constants are reduced and most stretching parameters increased when compared to fresh OTFTs stressed with similar pulses. Fig. 4(f) shows an increase in normalized mobility for all pulses. When compared to data of Fig. 4(c), the total increase in the mobility is similar; however, the stretching parameters are increased and the time constants decreased. This decrease in $\tau_{I_{ON}}$, τ_{V_T}, and τ_μ and increase in $\beta_{I_{ON}}$, β_{V_T} and β_μ indicates a faster, less dispersive mechanism in the aged transistors.

4.2. Discussion

In p-channel OTFTs the negative gate bias leads to channel formation (charge carrier accumulation) and thus causes a shift in V_T toward more negative values. If the field-effect mobility and the subthreshold slope did not change, this shift in $|V_T|$ would result in reduced on-state drain current (measured at $V_{GS} = V_{DS} = -2$ V in this case). The concurrent increase in the mobility, if any, would manifest itself as an increase in the on-state drain current, thus counteracting the effect of the threshold voltage. If μ rises faster than $|V_T|$, one may observe an overall increase in the on-state drain current. If $|V_T|$ increases faster than μ, then one would observe the typical reduction in the on-state drain current. However, if the rise in μ compensates the rise in $|V_T|$, a stable on-state drain current may result. Our results show that the on-state drain current of the aged transistors stabilizes around 500 s of the net bias stress. Yet, the threshold voltage and mobility keep rising, although their rise is slowing down. Therefore, the steady on-state drain current appears to result from μ compensating the $|V_T|$ shift.

In the initial stages of the DC bias stress an increase in the on-state drain current is observed for about 200 seconds. Previously similar increases were observed for OTFTs based on

DNTT and DNTT-derivatives and were attributed to a decrease in the contact resistance. [18] In fact, a reduction in the contact resistance can manifest itself as improved field-effect mobility and may be the driving factor for the mobility improvement observed here.

It has been reported that the DNTT/Au contact resistance is (1–6) $\times 10^2$ Ωcm. [32] This is one of the lowest reported values, surpassed only by DPh-DNTT/Au (56 Ωcm), DPh-DNTT/PFBT/Au (29 Ωcm) [33] and C_8-DNBDT-NW paired with Au/F_4TCNQ (47 Ωcm) [34]. Our transistors exhibit linear increase in I_D for small V_{DS} and the drain current saturation (see Figure 1(b)). However, close inspection of the saturation transfer characteristics shows that $\frac{\partial I_D^{1/2}}{\partial V_{GS}}$ goes through a maximum and a reduction of ~ 30% from the maximum value is observed when V_{GS} approaches –2 V. Consequently, in saturation, $I_D \sim (V_{GS} - V_T)^m$ where $m < 2$. The application of a procedure developed for amorphous silicon transistors [35] leads to $m \sim 1.7$. m exhibits slight increase with the increasing bias stress time, indicating a more ideal saturation behavior of the transistors with the progressing bias stress, for all bias stress conditions.

Fig. 5 shows the changes in the normalized on-state drain current, threshold voltage shift and normalized mobility versus the pulse period T or measurement/lapsed time, all for 1000 s of net bias stress. The reference points are the corresponding values before the bias stress. The pink symbol in Fig. 5(a) is an exception and represents the change in the drain current from its maximum value for DC bias stress. For shorter measurement time (smaller T) the value of the normalized on-state drain current after 1000 cycles decreases linearly with T, and stabilizes/reduces for $T = 60$ s. The value of the threshold voltage shift after 1000 cycles increases linearly with T and reduces/stabilizes for $T = 60$ s. However, the normalized drain current and $|\Delta V_T|$ at $T = 60$ s depend on the age of the transistors, leading to bigger changes for aged transistors. Finally, the value of the field-effect mobility after 1000 cycles increases

logarithmically with the measurement time and all transistors follow the same behavior regardless of their age. Consequently, the mobility improvement is associated with the measurement time and $T = 60$ s leads to the biggest improvement regardless of the transistor age.

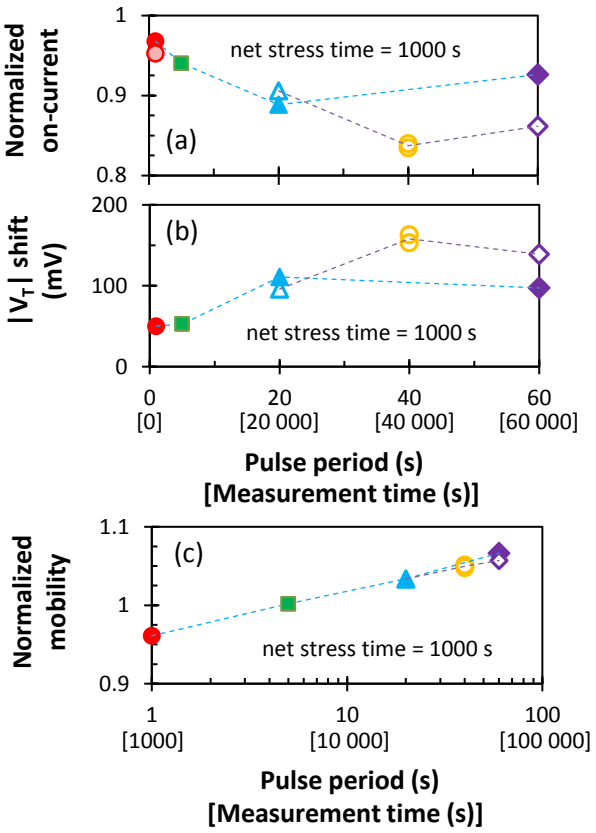


Figure 5. Normalized on-state drain current (a), threshold voltage shift (b) and normalized field-effect mobility (c) versus the pulse period T or measurement/lapsed time, for net bias stress of 1000 s. DC bias stress is represented as $T = 1$ s. Full and empty symbols correspond to the fresh and aged transistors. The light and dark blue dashed lines connect the measurements from fresh and aged transistors respectively. The pink symbol in (a) shows the change in drain current from its maximum value for DC bias stress.

5. Conclusions

We have shown how a low-voltage DNTT transistor with high on-state drain current can be implemented directly into the sensor to enhance its performance. A thermistor chosen to

respond to temperature changes was connected to the OTFT gate terminal. Two transistors with on-state drain currents of 61 and 126 μA at gate and drain voltages of −2 V were tested. The addition of the transistor increases the response to the temperature by a factor of ~5, all while limiting the supply voltage to less than –7 V. To achieve such an improvement, the transistor must operate in the saturation regime. In addition, the OTFT with higher on-state drain current exhibits stronger response to the changing temperature, resulting from higher voltage amplification.

We have also investigated the electrical stability of such transistors under DC and AC (on/off square pulses) bias stress. The chosen bias stress conditions forced the transistor either to operate in the saturation regime (desirable for the sensor) or be turned off. During each AC bias stress the transistor was repeatedly turned on for 1 s while the turn-off time was either 4, 19, 39 or 59 s. This resulted in 4 different AC waveforms with T = 5 s, 20 s, 40 s and 60 s. The on-state drain current of the transistor was measured; however, the changes in the threshold voltage, field-effect mobility, and subthreshold slope were also monitored. The total net stress time was 1000 s for the DC and all AC bias stresses. Under the DC bias stress, an initial increase in the on-state drain current was followed by a gradual decrease, leading to an overall drop of 3.2%. The $|V_T|$ exhibited a small increase and the mobility a small decrease. The net stress time of 1000 s led to a somewhat larger degradation of the on-state drain current for all AC pulses and the degradation proceeded faster and stabilized after about 500 s of net bias stress for aged transistors. For all transistors the drop in the on-state drain current and the shift in the threshold voltage reached maxima for medium values of T (T = 20 s and 40 s), thus leading to slightly reduced degradation for T = 60 s. Finally, the field-effect mobility gradually increased with T, leading to the largest enhancement for T = 60 s regardless of the transistor age. The value of the

normalized field-effect mobility after 1000 cycles increased logarithmically with the measurement time. Consequently, the mobility improvement is associated with the measurement time and the application of the intermittent voltages is beneficial.

The data set can be found at https://doi.org/10.15129/ ea954936-8a0b-46c0-b8b2-dbd7ced430f3.

Acknowledgements

This project has received funding from the European Union's Horizon 2020 research and innovation program under the Marie Skłodowska-Curie grant agreement No 734331. The authors wish to thank J. McCleary for selecting the components for the temperature sensor.

References

[1] D. Yin, Z.-Y. Chen, N.-R. Jiang, Y.-F. Liu, Y.-G. Bi, X.-L. Zhang, W. Han, J. Feng, H.-B. Sun, Highly Transparent and Flexible Fabric-Based Organic Light Emitting Devices for Unnoticeable Wearable Displays, Org. Electron. 76 (2020) 105494. https://doi.org/10.1016/j.orgel.2019.105494

[2] Z. Zhan, R. Lin, V.-T. Tran, J. An, Y. Wei, H. Du, T. Tran, W. Lu, A Paper-Carbon Nanotube-Based Wearable Pressure Sensor for Physiological Signal Acquisition and Soft Robotic Skin, ACS Appl. Mater. & Interfaces 9 (2017) 37921-37928. https://doi.org/10.1021/acsami.7b10820

[3] X. Fu, H. Dong, Y. Zhen, W. Hu, Solution-Processed Large-Area Nanocrystal Arrays of Metal–Organic Frameworks as Wearable, Ultrasensitive, Electronic Skin for Health Monitoring, Small 11 (2015) 3351-3356. https://doi.org/0.1002/smll.201402890

[4] M. Mizukami, S. I. Cho, K. Watanabe, M. Abiko, Y. Suzuri, S. Tokito, J. Kido, Flexible Organic Light-Emitting Diode Displays Driven by Inkjet-Printed High-Mobility Organic Thin-Film Transistors, IEEE Electron Dev. Lett. 39 (2018) 39-42. https://doi.org/10.1109/LED.2017.2776296

[5] S. Mandal, M. Banerjee, S. Roy, A. Mandal, A. Ghosh, B. Satpati, D. K. Goswami, Organic Field-Effect Transistor-Based Ultrafast, Flexible, Physiological-Temperature Sensors with Hexagonal Barium Titanate Nanocrystals in Amorphous Matrix as Sensing Material, ACS Appl. Mater. & Interfaces 11 (2019) 4193-4202. https://doi.org/10.1021/acsami.8b19051

[6] F. A. Viola, P. Cosseddu, S. Lai, A. Spanu, A. Bonfiglio, Flexible Temperature Sensors Based on Charge Modulated Organic Thin Film Transistors, IEEE Xplore 978-147998229-5 (2015) 278-281. Presented at 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), June 2015. https://doi.org/10.1109/PRIME.2015.7251389

[7] S. Jung, T. Ji, V. K. Varadan, Point-of-Care Temperature and Respiration Monitoring Sensors for Smart Fabric Applications, Smart Mater. Structures 15 (2006) 1872-1876. https://doi.org/10.1088/0964-1726/15/6/042

[8] T. Someya, Y. Kato, T. Sekitani, S. Iba, Y. Noguchi, Y. Murase, H. Kawaguchi, T. Sakurai, Conformable, Flexible, Large-Area Networks of Pressure and Thermal Sensors with Organic Transistor Active Matrixes, Proc. Natl. Acad. Sci. USA 102 (2005) 12321-12325. https://doi.org/10.1073/pnas.0502392102

[9] M. Zirkl, A. Sawatdee, U. Helbig, M. Krause, E. Kraker, D. Nilsson, D. Platt, P. Bodö, S. Bauer, G. Domann, B. Stadlober, An All-Printed Ferroelectric Active Matrix Sensor

Network Based on Only Five Functional Materials Forming a Touchless Control Interface Adv. Mater. 23 (2011) 2069-2074. https://doi.org/10.1002/adma.201100054

[10] X. Ren, K. Pei, B. Peng, Z. Zhang, Z. Wang, X. Wang, P. K. L. A. Chan, Low-Operating-Power and Flexible Active-Matrix Organic-Transistor Temperature-Sensor Array, Adv. Mater. 28 (2016) 4832-4838. https://doi.org/10.1002/adma.201600040

[11] D. Thuau, M. Abbas, S. Chambon, P. Tardy, G. Wantz, P. Poulin, L. Hirsch, I. Dufour, C. Ayela, Sensitivity Enhancement of a Flexible MEMS Strain Sensor by a Field-Effect Transistor in an All Organic Approach, Org. Electron. 15 (2014) 3096-4000. https://doi.org/10.1016/j.orgel.2014.08.063

[12] N. T. Tien, S. Jeon, D.-I. Kim, T. Q. Trung, M. Jang, B.-U. Hwang, K.-E. Byun, J. Bae, E. Lee, J. B.-H. Tok, Z. Bao, N.-E. Lee, J.-J. Park, A Flexible Bimodal Sensor Array for Simultaneous Sensing of Pressure and Temperature, Adv. Mater. 26 (2014) 796-804. https://doi.org/10.1002/adma.20130286

[13] A. Spanu, L. Pinna, F. Viola, L. Seminara, M. Valle, A. Bonfiglio, P. A. Cosseddu, Highly-Sensitive Tactile Sensor Based on Piezoelectric Polymer PVDF Coupled to an Ultra-Low Voltage Organic Transistor, Org. Electron. 36 (2016) 57-60. https://doi.org/10.1016/j.orgel.2016.05.034

[14] S. Jung, T. Ji, V. K. Varadan, Temperature Sensor Using Thermal Transport Properties in the Subthreshold Regime of an Organic Thin-Film Transistor, Appl. Phys. Lett. 90 (2007) 062105. https://doi.org/10.1063/1.2450646

[15] X. Wu, Y. Ma, G. Zhang, Y. Chu, J. Du, Y. Zhang, Z. Li, Y. Duan, Z. Fan, J. Huang, Thermally Stable, Biocompatible, and Flexible Organic Field Effect Transistors and Their

Application in Temperature Sensing Arrays for Artificial Skin, Adv. Functional. Mater. 25 (2015) 2138-2146. https://doi.org/10.1002/adfm.201404535

[16] J. Kim, J. Jang, K. Kim, H. Kim, S. H. Kim, C. E. Park, The Origin of Excellent Gate-Bias Stress Stability in Organic Field-Effect Transistors Employing Fluorinated-Polymer Gate Dielectrics, Adv. Mater. 26 (2014) 7241-7246. https://doi.org/10.1002/adma.201402363

[17] H. Sirringhaus, Reliability of Organic Field-Effect Transistors, Adv. Mater. 21 (2009) 3859-3873. https://doi.org/10.1002/adma.200901136

[18] S. Bisoyi, U. Zschieschang, M. J. Kang, K. Takimiya, H. Klauk, S. P. Tiwari, Bias-Stress Stability of Low-Voltage p-Channel and n-Channel Organic Thin-Film Transistors on Flexible Plastic Substrates, Org. Electron. 15 (2014) 3173–3182. https://doi.org/10.1016/j.orgel.2014.08.057

[19] W. L. Kalb, T. Mathis, S. Haas, A. F. Stassen, B. Batlogg, Organic Small Molecule Field-Effect Transistors with Cytop™ Gate Dielectric: Eliminating Gate Bias Stress Effects, Appl. Phys. Lett. 90 (2007) 092104. https://doi.org/10.1063/1.2709894

[20] X. Wei, J. Cao, A. Li, C. He, M. Liu, H. Meng, Enhancing the Electrical and Thermal Stability of Organic Thin-Film Transistors by Utilizing Fluorinated Polyimide and Silicon Dioxide Bilayer Gate Dielectric, J. Appl. Polymer Sci. 136 (2019) 47013. https://doi.org/10.1002/app.47013

[21] X. Jia, C. Fuentes-Hernandez, C.-Y. Wang, Y. Park, B. Kippelen, Stable Organic Thin-Film Transistors, Sci. Adv. 4 (2018), eaao1705. https://doi.org/10.1126/sciadv.aao1705

[22] M. Nikolka, I. Nasrallah, B. Rose, M. K. Ravva, K. Broch, A. Sadhanala, D. Harkin, J. Charmet, M. Hurhangee, A. Brown, S. Illig, P. Too, J. Jongman, I. McCulloch, J.-L. Bredas, H. Sirringhaus, High Operational and Environmental Stability of High-Mobility Conjugated

Polymer Field-Effect Transistors Through the Use of Molecular Additives, Nature Materials 16 (2017) 356-362. https://doi.org/10.1038/nmat4785

[23] U. Zschieschang, R. T. Weitz, K. Kern, H. Klauk, Bias Stress Effect in Low-Voltage Organic Thin-Film Transistors, Appl. Phys. A 95 (2009) 139-145. https://doi.org/10.1007/s00339-008-5019-8

[24] R. A., Street, M. L. Chabinyc, F. Endicott, B. Ong, Extended Time Bias Stress Effects in Polymer Transistors, J. Appl. Phys. 100 (2006) 114518. https://doi.org/10.1063/1.2398798

[25] U. Zschieschang, F. Ante, D. Kälblein, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, J. Blochwitz-Nimoth, H. Klauk, Dinaphtho[2,3-b:20,30-f]thieno [3,2-b]thiophene (DNTT) Thin-Film Transistors with Improved Performance and Stability, Org. Electron. 12 (2011) 1370–1375. https://doi.org/10.1016/j.orgel.2011.04.018

[26] A. Al Ruzaiqi, A. A. Ishaku, H. Gleskova, Organic Thin Film Transistors with Multi-Finger Contacts as Voltage Amplifiers, IEEE Access 6 (2018) 43770-43775. https://doi.org/10.1109/ACCESS.2018.2863043

[27] S. Hannah, J. Cardona, D. A. Lamprou, P. Šutta, P. Baran, A. Al Ruzaiqi, K. Johnston, H. Gleskova, Interplay Between Vacuum-Grown Monolayers of Alkylphosphonic Acids and the Performance of Organic Transistors Based on Dinaphtho[2,3-b:2′,3′-f]thieno[3,2-b]thiophene, ACS Appl. Mater. & Interfaces 8 (2016) 25405-25414. https://doi.org/10.1021/acsami.6b08426

[28] S. Gupta, S. Hannah, C. P. Watson, P. Šutta, R. H. Pederson, N. Gadegaard, H. Gleskova, Ozone Oxidation Methods for Aluminum Oxide Formation: Application to Low-Voltage Organic Transistors, Org. Electron. 21 (2015) 132-137. https://doi.org/10.1016/j.orgel.2015.03.007

[29] K. C. Chinnam, S. Gupta, and H. Gleskova, Aluminum Oxide Prepared by UV/Ozone Exposure for Low-Voltage Organic Thin-Film Transistors, J. Non-Crystalline Solids 358 (2012) 2512-2515. https://doi.org/10.1016/j.jnoncrysol.2012.01.016

[30] A. Al Ruzaiqi, B. Nikolov, R. L. Chen, H. Gleskova, Compact Modeling of Organic Transistors with Multi-Finger Contacts, IEEE Xplore 978-1-5386-9304-9/19 (2019). Presented at IEEE Int. Conf. on Flexible and Printable Sensors and Systems (IEEE FLEPS 2019). https://doi.org/10.1109/FLEPS.2019.8792299

[31] O. Marinov, M. Deen, U. Zschieschang, H. Klauk, Organic Thin-Film Transistors: Part I - Compact DC Modeling, IEEE Trans. Electron Dev. 56 (2009) 2952-2961. https://doi.org/10.1109/TED.2009.2033308

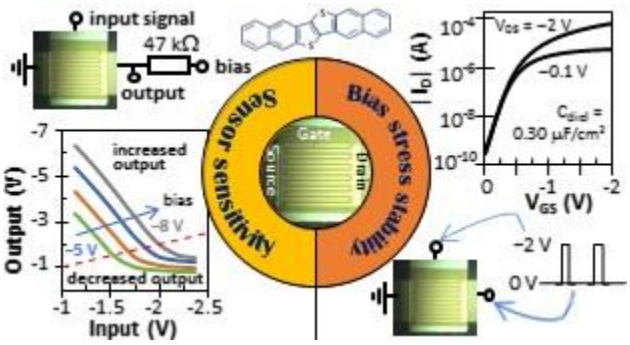
[32] M. Waldrip, O. D. Jurchescu, D. J. Gundlach, E. G. Bittle, Contact Resistance in Organic Field-Effect Transistors: Conquering the Barrier, Adv. Func. Mater. 30 (2020) 1904576. https://doi.org/10.1002/adfm.201904576

[33] J. W. Borchert, B. Peng, F. Letzkus, J. N. Burghartz, P. K. L. Chan, K. Zojer, S. Ludwigs, H. Klauk, Small Contact Resistance and High-Frequency Operation of Flexible Low-Voltage Inverted Coplanar Organic Transistors, Nat. Commun. 10 (2019) 1199. https://doi.org/10.1038/s41467-019-09119-8 [34] A. Yamamura, S. Watanabe, M. Uno, M. Mitani, C. Mitsui, J. Tsurumi, N. Isahaya, Y. Kanaoka, T. Okamoto, J. Takeya, Wafer-Scale, Layer-Controlled Organic Single Crystals for High-Speed Circuit Operation, Sci. Adv. 4 (2018) eaao5758. https://doi.org/10.1126/sciadv.aao5758

[35] A. Ortiz-Conde, A. Cerdeira, M. Estrada, F. J. G. Sanchez, R. Quintero, A Simple Procedure to Extract the Threshold Voltage of Amorphous Thin-Film MOSFETs in the

Saturation Region, Solid-State Electron. 45 (2001) 663-667.

https://doi.org/10.1016/S0038-1101(01)00123-X



Graphical abstract.