COMPARATIVE ANALYSIS OF FAULT DETECTION AND CLASSIFICATION TECHNIQUES FOR HVDC GRIDS PROTECTION

Vinícius A. Lacerda[1,3], David Campos-Gaona[1], Rafael Pena-Alzola[1], Renato M. Monaro[2], Denis V. Coury[3], Olimpo Anaya-Lara[1]*

[1]*Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, United Kingdom.*
[2]*Department of Electric Energy and Automation Engineering, Polytechnic School, University of São Paulo, São Paulo, Brazil.*
[3]*Department of Electrical and Computer Engineering, São Carlos School of Engineering, University of São Paulo, São Carlos, Brazil.*
**vinicius.albernaz.freitas@usp.br*

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Abstract

Dealing with high short-circuit currents with a fast rise rate in Voltage Source Converters (VSCs) still poses as a challenge for High Voltage Direct Current (HVDC) multiterminal system (MTDC) reliability. Several fault detection algorithms have been proposed for multiterminal VSC-HVDC grids, such as undervoltage, overcurrent and their respective time derivatives. This work investigates their performance in terms of speed, sensitivity and correctness concerning classification. Tests were conducted by simulating pole-to-pole and pole-to-ground faults in different locations and fault resistances in a four-terminal VSC-HVDC grid. The results confirmed that voltage-based algorithms performed better than current-based algorithms in most cases. Furthermore, a voltage ratio method is proposed to increase fault classification performance during low-resistance faults.

1 Introduction

The increase in renewable generation in the energy mix, as well as the need for controllability and interconnection, were the drivers for the increasing use of High Voltage Direct Current (HVDC) technology in transmission systems [1]. Among the converter topologies of HVDC systems, the Voltage Source Converter (VSC) is seen as an enabling technology for interconnecting asynchronous sources in a liberalised market [2].

However, high short-circuit currents of VSC converters still pose as a challenge for HVDC grid reliability [3]. In case of a fault in a VSC-HVDC system, the discharge of the converter capacitors leads to high magnitude short-circuit currents [4]. Short-circuit currents, which rise sharply, can damage the DC grid components and impose high current supportability, energy dissipation and breaking time requirements on the DC circuit breakers [5], [6].

The longer the time to interrupt the fault, the more energy the surge arresters have to dissipate, which increases the cost of circuit breakers. If the DC voltage drops below 80 % of the nominal value, the converters connected to the HVDC grid are blocked [4]. Hence, research efforts have focused on reducing the total breaking time of DC breakers [7], which is the sum of the protection algorithm fault identification time and the breaker opening time. In general, DC faults should be cleared within 3-5 ms to avoid tripping of VSC converters [4]. As the opening time of the hybrid breaker is 2-5 ms [8], protection algorithms need to detect and locate short-circuits in a very short time.

Various fault-detecting algorithms were proposed for VSC-HVDC systems, which are mostly adaptations from traditional AC transmission systems, such as overcurrent, undervoltage, and derivative-based algorithms [9], [10]. This paper investigates their performance in terms of speed, sensitivity and correctness concerning classification.

This paper is organised as follows. Section 2 describes the MTDC system modelled and analysed fault simulations. In Section 3, the methodology is described, showing tested techniques and test cases. The results are shown in Section 4, and the conclusions are drawn in Section 5.

2. MTDC Modelling and Fault Simulations

2.1 Test System

The test system was based on [11], a symmetric monopole Modular Multilevel Converter (MMC)-based multiterminal HVDC system with four terminals (Fig. 1). The system was simulated in PSCAD software. The system parameters are summarised in Table 13, in the Appendix. It should be noted

that a DC bus capacitor was connected to each terminal to provide DC voltage measurements and grounding.

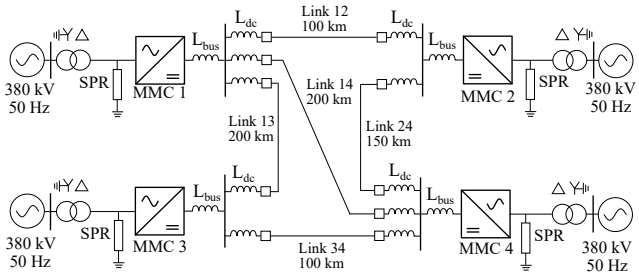


Fig. 1 MTDC system single line diagram. Adapted from [11].

The converters were modelled using the detailed Thévenin equivalent model [12]. All DC cables were modelled using the frequency-dependent model. The cable parameters were based on [11]. The armour and sheath were assumed to be ideally grounded, and soil resistivity was assumed as 1 Ωm. The converters' arms overcurrent protection was set to 2 p.u = 3.87 kA for MMCs 1, 2 and 3, and 5.16 kA for MMC 4. The pick-up time was 0.1 ms.

MMCs 1, 2 and 3 performed active power control, with $P_{MMC1} = 700$ MW, $P_{MMC2} = 700$ MW and $P_{MMC3} = -600$ MW. The MMC 4 performed DC grid voltage control with $V_{dc} = 640$ kV. All MMCs reactive power set points were -100 Mvar. The circulating current control was implemented using proportional-resonant (PR) controllers.

The difference between the model in Fig. 1 and the model in [11] was the addition of a star-point reactor (SPR) between the transformer and the converter. The star-point reactor is used to provide a ground path in the converters' AC side and to rebalance any voltage unbalances due to control or monopole faults that could cause DC current flow in the transformers [13]. The SPR phase inductance (L_{spr}) is chosen to provide a low-impedance path for the DC current and a high-impedance path for the AC current [14]. The star-point reactor resistor (R_{spr}) is used to avoid resonance between the conductor-to-ground capacitance of the DC voltage intermediate circuit and the inductance of the star-point reactor [14]. Until the present date, no design procedure was found for the SPR. Hence, as the modelled system topology, voltage levels and power ratings were similar to the stations in the INELFE project (France-Spain Electrical Interconnection) and the same values were adopted for the SPR [15] (see Table 13).

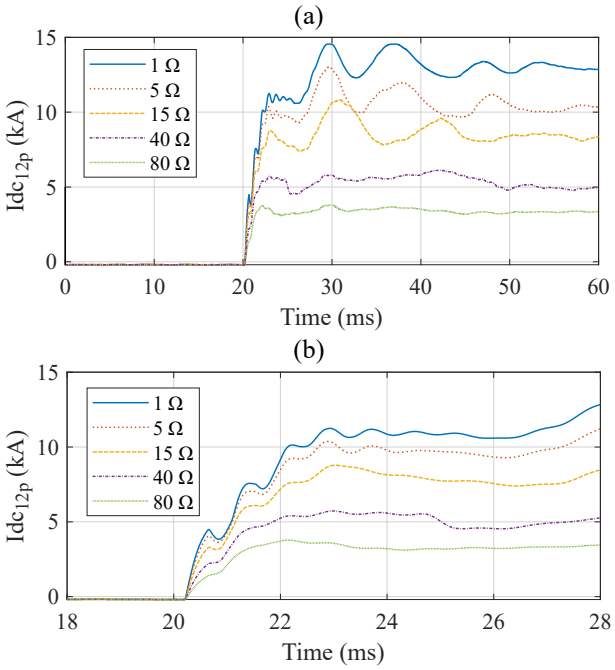
2.2 Fault Cases

Several fault cases were simulated in different scenarios. Fault type, fault location and fault resistance were varied, resulting in a total of 1,236 cases, summarised in Table 1. For all faults, the following variables were acquired: positive and negative pole voltage of all connections to all terminals, positive and negative current of all links connecting all terminals, the converters' block state and the SPR current and power in all MMCs.

Table 1 Summary of fault cases.

Fault parameter	**Values**
Fault type 1	Pole-to-Pole
Fault type 2	Positive Pole-to-ground
Fault resistances	1 Ω, 5 Ω, 10 Ω, 20Ω, 40 Ω, 80 Ω
Link 12 locations	5, 10, 15, …, 95 km
Link 13 locations	5, 15, 25, …, 195 km
Link 14 locations	5, 10, 15, …, 195 km
Link 24 locations	5, 15, 25, …, 145 km
Link 34 locations	5, 15, 25, …, 95 km
Total	**1,236 cases**

Fig. 2 shows the DC current and DC voltage for a fault at Link 12, 40 km from MMC 1 for different fault resistances, occurring at $t = 20$ ms. By analysing Fig. 2, it can be observed that the lower fault resistances implied greater fault currents and smaller voltage levels, both before and after converter blocking. The converter was blocked after 2.5 ms for 1 Ω fault resistance, 2.6 ms for 5 Ω, 3.2 ms for 15 Ω, 4.6 ms for 40 Ω and was not blocked for 80 Ω fault resistance. In Fig. 2c, a waviness can be noted in the current between 20 ms and 24 ms. It can also be observed that the current starts rising a short period after 20 ms. This is mainly due to the travelling wave effect, which can be seen more clearly in the voltage in Fig. 2d.



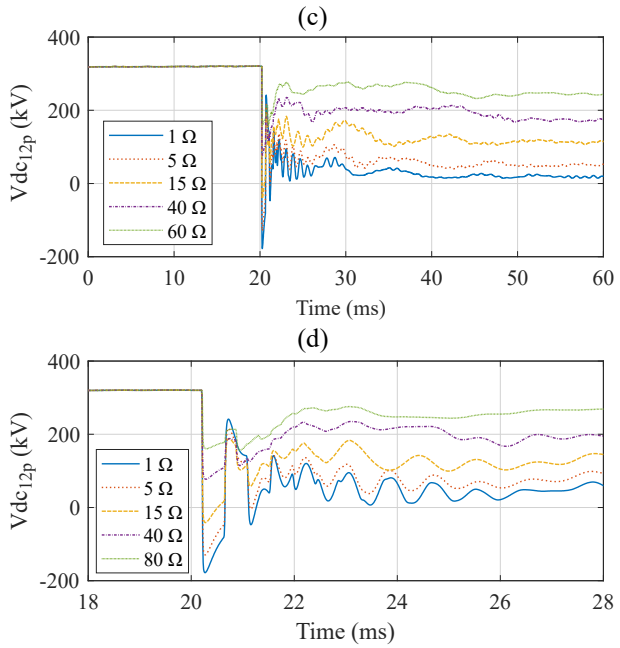


Fig. 2 Fault at the positive pole of Link 12 with different fault resistances: a) DC current, b) DC voltage, c) DC current in detail, d) DC voltage in detail.

3 Methodology

A selection of traditional VSC-HVDC protection algorithms was tested using the fault cases described in Section 2.

For the sake of simplicity, only one circuit breaker (DCCB at Link 14 at MMC 1 terminal) and its measurements were used in the tests. The variables used in the tests were the DC currents and voltages at the positive and negative poles (I_{dc14p}, I_{dc14n}, V_{dc14p} and V_{dc14n}).

The algorithms' speed, sensitivity and selectivity were analysed using the aforementioned cases. In order to approximate the simulated cases from real-world applications, measurement errors of white noise were introduced into the variables with SNR = 40 dB, and then filtered using a fourth-order Butterworth filter. The voltage and current waveforms were filtered using a cutting frequency of 2 kHz. The sampling frequency in this protection experiment was 50 kHz.

Fault detection algorithms aim to detect any fault in the DC grid, regardless of its location. Fault classification aims to detect what type of fault it is: positive pole-to-ground, negative pole-to-ground or pole-to-pole.

Traditional fault detection algorithms include overcurrent, undervoltage, current derivative and voltage derivative [16], [17] and [18]. These algorithms can also operate together, using AND logic and can also be used to classify the fault type. In this study, the tested algorithms were:

- *Overcurrent*: if $I_{dc} > I_{max}$, detect fault.
- *Undervoltage*: if $V_{dc} < V_{min}$, detect fault.
- *Current derivative*: if $\left|\frac{dI_{dc}}{dt}\right| > \frac{\Delta I_{max}}{\Delta t}$, detect fault.
- *Voltage derivative*: if $\left|\frac{dV_{dc}}{dt}\right| > \frac{\Delta V_{max}}{\Delta t}$, detect fault.
- *Overcurrent and undervoltage*: if $I_{dc} > I_{max}$ AND $V_{dc} < V_{min}$, detect fault.
- *Overcurrent and voltage derivative*: if $I_{dc} > I_{max}$ AND $\left|\frac{dV_{dc}}{dt}\right| > \frac{\Delta V_{max}}{\Delta t}$, detect fault.
- *Undervoltage and current derivative*: if $V_{dc} < V_{min}$ AND $\left|\frac{dI_{dc}}{dt}\right| > \frac{\Delta I_{max}}{\Delta t}$, detect fault.
- *Current derivative and voltage derivative*: if $\left|\frac{dI_{dc}}{dt}\right| > \frac{\Delta I_{max}}{\Delta t}$ AND $\left|\frac{dV_{dc}}{dt}\right| > \frac{\Delta V_{max}}{\Delta t}$ detect fault.

Where, I_{dc}, V_{dc}, $\left|\frac{dI_{dc}}{dt}\right|$ and $\left|\frac{dV_{dc}}{dt}\right|$ are the DC current, voltage, and their time derivatives, respectively. And I_{max}, V_{min}, $\frac{\Delta I_{max}}{\Delta t}$, and $\frac{\Delta V_{max}}{\Delta t}$ are the respective pre-defined thresholds. All thresholds were given in p.u. The base DC voltage was 320 kV (pole-to-ground voltage) and the base DC current was 1.45 kA.

To increase the robustness of the algorithms against outliers, when the variable (current, voltage or derivative) crossed the defined threshold, a counter was incremented. When the variable did not cross the threshold, the counter was decremented. When the counter hit three counts, the fault flag was raised.

The data series consisted of 5 ms pre-fault and 10 ms post-fault. After the fault was detected in one pole, the algorithm waited for 1.0 ms for a possible second faulted pole before ending the loop. When the fault was detected in two poles, the detection delay was assumed to be the instant when the last flag was raised. The travelling wave delay was compensated.

4 Results

Tables 2 to 9 summarise the performance of all tested algorithms. For all algorithms, a range of four different thresholds were considered. In each table, the "Threshold" column indicates the threshold used to detect the fault, the "Correct" column shows the cases where the fault was detected and classified correctly; the "Incorrect" column shows the cases where the fault was detected but was not classified correctly; the "False trip" column shows the cases where the protection tripped while the system was still in normal operation. The last column shows the average time delay to the fault detection of the respective cases. The tables were displayed in decreasing order performance from the algorithm that detected the most number of faults to the algorithm that detected the least number of faults. The time delay was computed only for the correct detections.

Table 2 Undervoltage performance.

Threshold	Correct	Incorrect	False Trip	Undetected	Delay
0.85 p.u	100 %	0.0 %	0.0 %	0.0 %	0.7 ms
0.80 p.u	100 %	0.0 %	0.0 %	0.0 %	0.9 ms
0.75 p.u	99.4 %	0.4 %	0.0 %	0.2 %	1.1 ms
0.70 p.u	94.9 %	0.0 %	0.0 %	5.1 %	1.4 ms

Table 3 Voltage derivative performance.

Threshold	Correct	Incorrect	False Trip	Undetected	Delay
0.25 p.u/ms	87.9 %	4.5 %	1.9 %	5.7 %	0.4 ms
0.50 p.u/ms	64.1 %	1.8 %	0.0 %	34.1 %	0.4 ms
0.75 p.u/ms	40.9 %	0.9 %	0.0 %	58.3 %	0.2 ms
1.00 p.u/ms	37.9 %	0.0 %	0.0 %	62.1 %	0.1 ms

Table 4 Undervoltage and Current Derivative performance.

Threshold	Correct	Incorrect	False Trip	Undetected	Delay
0.85 p.u & 0.5 p.u/ms	85.0 %	0.3 %	0.0 %	14.7 %	0.8 ms
0.80 p.u & 1.0 p.u/ms	65.8 %	1.0 %	0.0 %	33.3 %	0.9 ms
0.75 p.u & 1.5 p.u/ms	43.5 %	0.9 %	0.0 %	55.6 %	0.4 ms
0.70 p.u & 2.0 p.u/ms	35.0 %	0.5 %	0.0 %	64.6 %	0.3 ms

Table 5 Current Derivative performance.

Threshold	Correct	Incorrect	False Trip	Undetected	Delay
0.5 p.u/ms	81.5 %	5.7 %	4.4 %	8.4 %	0.6 ms
1.0 p.u/ms	77.6 %	0.6 %	0.1 %	21.7 %	0.6 ms
1.5 p.u/ms	63.2 %	0.3 %	0.0 %	36.5 %	0.3 ms
2.0 p.u/ms	52.8 %	0.6 %	0.0 %	46.7 %	0.3 ms

Table 6 Voltage Derivative and Current Derivative performance.

Threshold	Correct	Incorrect	False Trip	Undetected	Delay
0.25 & 0.5 p.u/ms	81.1 %	2.9 %	0.0 %	15.9 %	0.6 ms
0.50 & 1.0 p.u/ms	56.6 %	1.0 %	0.0 %	42.5 %	0.3 ms
0.75 & 1.5 p.u/ms	36.9 %	1.0 %	0.0 %	62.1 %	0.2 ms
1.00 & 2.0 p.u/ms	30.6 %	0.5 %	0.0 %	68.9 %	0.2 ms

Table 7 Overcurrent and Undervoltage performance.

Threshold	Correct	Incorrect	False Trip	Undetected	Delay
1.1 & 0.85 p.u	74.4 %	0.1 %	0.0 %	25.6 %	1.4 ms
1.3 & 0.80 p.u	64.7 %	0.2 %	0.0 %	35.1 %	1.5 ms
2.0 & 0.75 p.u	47.4 %	0.0 %	0.0 %	52.6 %	1.6 ms
2.7 & 0.70 p.u	35.1 %	0.2 %	0.0 %	64.6 %	1.4 ms

Table 8 Overcurrent performance.

Threshold	Correct	Incorrect	False Trip	Undetected	Delay
1.1 p.u	74.0 %	1.1 %	0.0 %	24.8 %	1.5 ms
1.3 p.u	65.0 %	0.1 %	0.0 %	35.0 %	1.6 ms
2.0 p.u	47.7 %	0.0 %	0.0 %	52.3 %	1.6 ms
2.7 p.u	36.2 %	0.0 %	0.0 %	63.8 %	1.4 ms

Table 9 Overcurrent and Voltage Derivative performance.

Threshold	Correct	Incorrect	False Trip	Undetected	Delay
1.1 p.u & 0.25 p.u/ms	59.7 %	3.4 %	0.0 %	36.9 %	1.1 ms
1.3 p.u & 0.50 p.u/ms	42.6 %	0.8 %	0.0 %	56.6 %	1.0 ms
2.0 p.u & 0.75 p.u/ms	27.3 %	0.6 %	0.0 %	72.1 %	1.0 ms
2.7 p.u & 1.0 p.u/ms	21.1 %	0.4 %	0.0 %	78.5 %	1.2 ms

From the results shown, it can be observed that the algorithms that used the DC voltage as the protection variable correctly detected a greater number of faults and operated faster than the algorithms based on the DC current. This happened due to the voltage being maintained by capacitors, which have low inertia. Thus, as soon as a fault happens, the voltage drops significantly. This effect can easily be seen when fault current limiting reactors are placed in each terminal. In this case, the current will be limited and the inductor will delay the converters' voltage to be transferred to the pole where the fault is.

4.1 Influence of fault resistance

It is well known that in AC systems, the fault resistance (R_f) impacts the fault detection significantly. In this subsection, this impact is analysed in the tested DC protections.

Tables 9, 10 and 11 summarise the performance of Voltage Derivative, Current Derivative and Overcurrent, respectively, for their respective first threshold. Undervoltage correctness was not affected by the fault resistance, but its operation was delayed. For example, with $R_f = 1\ \Omega$, the average delay was 0.5 ms, and with $R_f = 80\ \Omega$, the average delay was 1.2 ms.

Table 10 Influence of R_f on Current Derivative performance. Threshold = 0.5 p.u/ms.

R_f	Correct	Incorrect	False Trip	Undetected	Delay
1 Ω	88.3 %	1.0 %	0.0 %	10.7 %	0.6 ms
5 Ω	84.5 %	1.0 %	0.5 %	14.6 %	0.6 ms
10 Ω	82.5 %	1.0 %	0.0 %	16.5 %	0.6 ms
20 Ω	82.5 %	1.0 %	0.0 %	16.5 %	0.6 ms
40 Ω	75.2 %	0.0 %	0.0 %	24.8 %	0.3 ms
80 Ω	52.4 %	0.0 %	0.0 %	47.6 %	0.2 ms

Table 11 Influence of R_f on Overcurrrent performance. Threshold = 1.1 p.u.

R_f	Correct	Incorrect	False Trip	Undetected	Delay
1 Ω	87.4 %	0.5 %	0.0 %	12.1 %	1.4 ms
5 Ω	85.0 %	0.0 %	0.0 %	15.0 %	1.6 ms
10 Ω	76.7 %	0.0 %	0.0 %	23.3 %	1.6 ms
20 Ω	56.8 %	0.0 %	0.0 %	43.2 %	1.1 ms
40 Ω	46.1 %	0.0 %	0.0 %	53.9 %	0.8 ms
80 Ω	37.9 %	0.0 %	0.0 %	62.1 %	0.3 ms

As can be observed in the tables, while the fault resistance had a minor impact on the undervoltage algorithm, it significantly impacted the performance of current-based algorithms. The greater the fault resistance, the greater the undetected faults. When the resistance between the converter and the fault is high, the maximum fault current reduces, but the initial voltage drop due to the first travelling wave is still high (compare Fig. 2b and Fig. 2d). Therefore, in high-resistive fault cases, the protection that uses the current may not trip while the protection that uses the voltage may trip but with a slightly greater delay. Another result was that wrong fault classifications were higher for low impedance faults in the performance of the three algorithms. This occurred because a fault in one pole also affects the other pole slightly. Fig. 3 shows one case of incorrect classification.

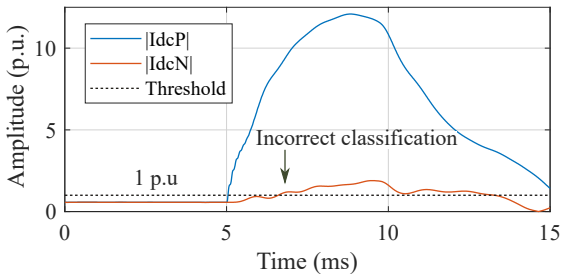


Fig. 3 Absolute value of DC currents. Overcurrent threshold of 1 p.u.

4.2 Increasing pole classification correctness

A possible solution for the incorrect pole classification would be adding a new variable to the existing protection algorithms. The role of this variable is to indicate clearly the faulted pole. In this work, the ratio between positive and negative voltages is used. It is known that, in pole-to-ground faults, the voltage in the faulted pole will collapse and the voltage in the healthy pole will increase in magnitude [19], whereas in a pole-to-pole faults the symmetry will be maintained. Hence, this voltage ratio, when operating in conjunction with fault detection algorithms, helps to discriminate between positive pole-to-ground (PG), negative pole-to-ground (NG) and pole-to-pole (PP) faults. A first attempt would be to divide positive and negative voltages. In order to avoid division by zero when one of the voltages collapses, 1 is summed with the values in p.u resulting in the ratio $r_v = \frac{|V_{dcP}+1|}{|V_{dcN}+1|}$. When $r_v > 1$, the magnitude of the positive pole voltage is greater than the magnitude of the negative voltage, indicating negative pole-to-ground fault. Conversely, when $r_v < 1$, it indicates a positive pole-to-ground fault and $r_v = 1$ indicates a pole-to-pole fault. This is depicted in Fig. 4.

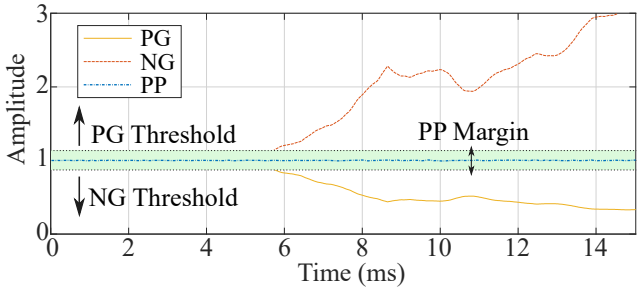


Fig. 4 Ratio $\frac{|V_{dcP}+1|}{|V_{dcN}+1|}$ and example of possible ratio threshold.

To increase robustness, a safe margin for r_v can be used (PP margin in Fig. 4). A safe margin of 0.95-1.05 for r_v (pole-to-pole fault margin) was used and the r_v parameter was added to the current derivative algorithm, the one with the greatest incorrect classifications. The results are shown in Table 12.

Table 12 Current Derivative performance with proposed voltage ratio.

Threshold	Correct	Incorrect	False Trip	Undetected	Delay
0.5 p.u/ms	90.0 %	0.0 %	0.2 %	9.8 %	0.6 ms
1.0 p.u/ms	77.7 %	0.0 %	0.0 %	22.3 %	0.6 ms
1.5 p.u/ms	63.2 %	0.0 %	0.0 %	36.8 %	0.4 ms
2.0 p.u/ms	52.5 %	0.0 %	0.0 %	47.5 %	0.3 ms

Comparing Table 5 to Table 12, it can be observed that using the voltage ratio threshold eliminated all incorrect classifications and reduced the number of false trips.

5 Conclusion

Dealing with short-circuit currents still remains a challenge in VSC-HVDC systems. The longer the time to interrupt the fault, the more energy the surge arresters have to dissipate, imposing stringent requirements to DC circuit breakers. In order to rapidly detect the fault, several fault detection algorithms were proposed for multiterminal VSC-HVDC grids, such as undervoltage, overcurrent and their respective time derivatives. This work investigated their performance in terms of speed, sensitivity and correct classification.

The results showed that voltage-based algorithms performed better than current-based algorithms. This happened because when the resistance between the converter and the fault is high, the maximum fault current reduces, but the initial voltage drop due to the first travelling wave is still high. Furthermore, to reduce the number of incorrect fault classifications in low-resistance faults, a voltage ratio between the positive and negative pole was proposed. The proposed ratio increased the correctness of fault classification.

The comparative analysis performed helps to understand the performance of DC fault detection algorithms used in MTDC systems and indicates the relationship between the variables used in the protection and the fault phenomena.

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7 Appendix

The HVDC system parameters are summarized in Table 13.

Table 13 Test system parameters.

	MMC 1,2,3	MMC 4	
AC Grid			
AC reactance	17.75	13.34	Ω
AC resistance	1.77	1.34	Ω
Transformer			
Power	900	1200	MVA
Leakage reactance	0.15	0.15	p.u.
Winding voltages	400/400	400/400	kV/kV
Converter			
Voltage	380	380	kV
Power	900	1200	MVA
SM per arm (N)	50	50	-
SM capacitance	1465	1950	μF
Arm inductance	84.8	63.6	mH
SM ON-state resistance	0.0177	0.0134	Ω
SM OFF-state resistance	100	100	MΩ
DC Bus			
DC Bus reactor (L_{bus})	10	10	mH
DC capacitor	2.5	2.5	μF
DC line reactor (L_{dc})	30	50	mH
Star-point reactor			
Phase inductance (L_{spr})	5000	5000	H
Grounding resistance (R_{spr})	5	5	kΩ

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