

Integration of an LED/SPAD Optical Wireless Transceiver with CubeSat On-board Systems

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Abstract—We demonstrate integration of Cube-Sat on-board equipment with a field programmable array gate-based light emitting diode/single photon avalanche photodiode transceiver using an inter-integrated circuit protocol.

Keywords—satellite communications, optical camera communications, discrete pulse amplitude modulation, LED array.

I. INTRODUCTION

Optical intersatellite links (OISL's) are a promising alternative to their microwave counterparts providing higher bandwidth, and efficiency in terms of antenna size, weight, and power consumption (SWaP) [1]. Hence, OISL is an ideal choice for nano- and pico-satellites, in particular, where low SWaP equipment is essential. Laser transmitters (Tx's) with a very narrow beam divergence and high gain are well studied in the context of intersatellite communications [2]. However, most laser-based communication systems have a SWaP footprint that is challenging for small satellites, i.e., <10 kg. Moreover, pointing error is a major issue in laser-based transceivers [3]. Light emitting diodes (LEDs) are a low SWaP alternative that have the additional benefit of a larger divergence angle, thus relaxing pointing accuracy requirements[4]. However, large divergence imposes a high geometrical attenuation, therefore a low received power for a limited transmit power, especially in long link spans, e.g., > 1 km. To compensate for this loss, LED/single photon avalanche diode (SPAD) transceivers have been investigated and show promising capabilities, e.g., a data rate of 100 Mbps at a sensitivity of 55.2 dBm [5]. An important remaining challenge is the integration of the hardware with on-board systems.

In this paper, we present a transceiver system, where LED and SPAD components are connected to a single field programmable gate array (FPGA) that manages symbol-level clock synchronization and frame-level alignment, which is in turn controlled by an on-board computer (OBC) through inter-integrated circuit (I²C) protocol. Frame-level and symbol-level synchronization are achieved through a dedicated protocol that has been specifically designed for on-off-keying (OOK) and single photon detection. An image taken with an on-board imaging system has been transmitted to demonstrate the transceiver functionality and its use in conjunction with other payload systems.

II. SYSTEM MODEL

Figure 1(a) illustrates the schematic system model used in this work. On-board components such as imaging systems and the transceiver FPGA are controlled by the OBC through the I²C protocol. The FPGA translates between the I²C protocol and the optical transmission protocol by which the data are transmitted using a single LED through a wireless visible light channel and received by the SPAD detector of the second satellite. Received data are passed to the FPGA for decoding and data extraction and the OBC of the second satellite receives and stores the image. The optical transmission protocol employs OOK, where payload data are transferred in frames of 32-bit length. Between any two frames, a constant 6-bit pilot signal "001101" is repeated to enable symbol- and frame-level synchronization. Clock synchronization on the receiver end is efficiently achieved by employing fix point math on the FPGA and evaluating a number of N consecutive frames, where a particularly simple implementation is possible if N is a power of 2. Furthermore, the protocol sends data in blocks of a fixed length of frames, where the start of each block is marked by a frame with all bits on. The pilot signal is continuously being sent between blocks to maintain link synchronization. In the I²C protocol developed in this work, the OBC software and FPGA firmware have been developed to implement the I²C master and slave for this protocol, respectively. The parameters of communication are controlled using a number of I²C registers. Two registers are used for sending or receiving an entire block of data. Packing/unpacking the data to/from blocks is performed by the OBC software. Further registers are used to set parameters such as block length, data rate (given as a 32-bit clock divider on a 100 MHz clock), or reset. Other registers are used for status indication, such as whether receiver (Rx) has stable clock synchronization, or fill status of the Rx/Tx buffer memories on the FPGA.

III. RESULTS

In order to evaluate the performance of the system, an experimental setup containing a NanoBed flat-pack cube-sat test-bed, a Xilinx Spartan 6 FPGA, a single 450-nm LED with digital on-off modulation through a p-channel metal-oxide semiconductor field effective transistor (MOSFET), and a SPCM20 Thorlabs single photon counter was used, see Fig. 1(b). In this work, the N was set to 16 and the corresponding clock synchronization circuit uses about 4500 flip-flops and 8000 look-up tables on the FPGA. The bit rate was set to 400 kb/s and the block length was set to 4 frames. In order to assess the performance of synchronization algorithm, at

each received power the number of times the Tx and Rx locked was obtained by averaging over 10^5 attempts repeated 10 times, i.e., 10^6 attempts in total. Figure 2(a) depicts the average success rate of the phase locking between Tx and Rx as a function of average received photons per set bit. The results show that to have a reliable transmission, a photon count of 50 photons per set bit is required. Note, if the phase is not locked, the packet is lost and hence bit error rate increases. A useful strategy for this situation is that the Rx sends an acknowledgement to the Tx for each packet received. Therefore, if an acknowledgement is not received, Tx retransmits the packet. Next, we captured an image of a “ μ LED” text object, see Fig. 2(b), placed 0.5 m away from the on-board camera. Due to memory limitations of the OBC, a thumbnail image with a resolution of 41×101 was used, which contained some distortions caused by the camera module’s thumbnail creation process, see Fig. 2(c). The data were saved in raw bit format, transmitted over the visible light channel, and saved in the memory of the OBC. Figure 2(d) shows the received image at the receiver side, where the root mean square error 2.1% of the image dynamic range (8 bit). Note, in the system used in this work, the image is not encoded with error correction codes. Moreover, since these images are thumbnail, the imaging system creates some distortions, e.g., the diagonal lines across the images. In order to improve the quality of received image, forward error correction algorithms can be used.

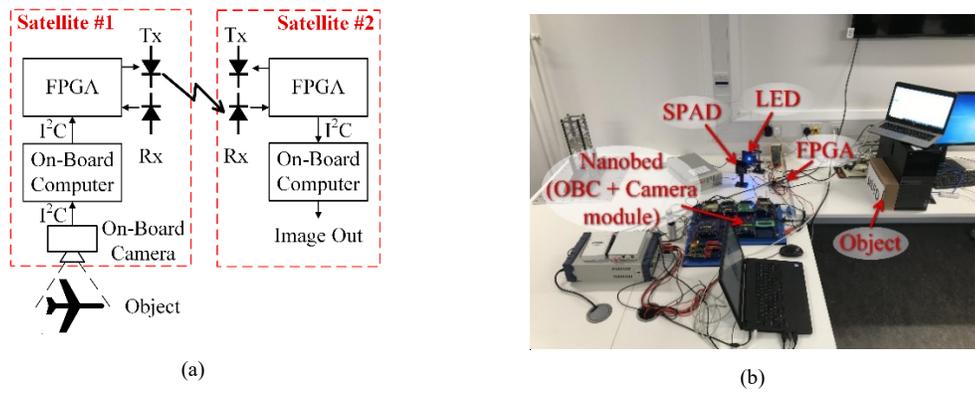


Fig. 1. (a) System block diagram and (b) experimental test-bed.

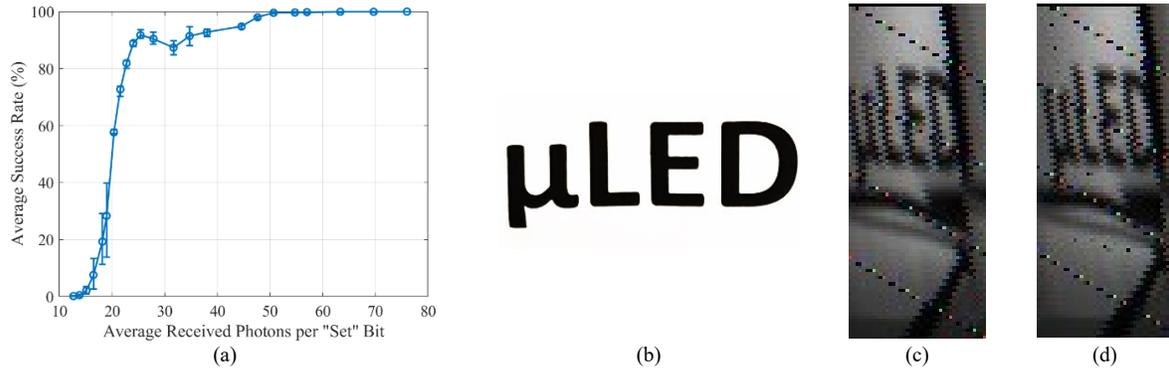


Fig. 2. (a) Average synchronization success rate as a function of average received photons per set bit, (b) text object (c) transmitted image, and (d) received image.

IV. CONCLUSION

In this paper, we presented integration of FPGA controlled LED/SPAD transceiver with on-board unit using I2C protocol. We showed that in the proposed system, 50 photons are needed to be received per set bit to establish a lossless link. Moreover, we demonstrated image transfer over visible light channel.

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