Partially Reconfigurable TVWS Transceiver for Use in UK and US Markets

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***Abstract*—With more and more countries opening up sections of unlicensed spectrum for use by TV White Space (TVWS) devices, the prospect of building a device capable of operating in more than one world region is appealing. The difficulty is that the locations of TVWS bands within the radio spectrum are not globally harmonised. With this problem in mind, the purpose of this paper is to present a TVWS transceiver design which is capable of being reconfigured to operate in both the UK and US spectrum. We present three different configurations: one covering the UK TVWS spectrum and the remaining two covering the various locations of the US TVWS bands.**

I. Introduction

TVWS devices are subject to a number of requirements which are in place to protect incumbent users. These restrictions are strictly governed in the US by the Federal Communications Commission (FCC) Office of Engineering and Technology (OET), with the regulations for the UK currently being put in place by OFCOM. The spectral mask details permissible interference levels that have been determined to protect incumbent users. This is outlined in Fig. 1 where -55dB leakage into adjacent frequency bands and -69dB interference into next-adjacent channels is permitted [1].

These strict spectral requirements mean that Orthogonal Frequency Division Multiplexing (OFDM) - currently commonplace in most wireless standards - is ill-suited. Therefore, filter bank based transceivers, many of which appeared before the introduction of OFDM [2]–[5], have recently experienced a renaissance in a number of communications areas [6]–[8]. This is due to filter bank techniques offering greatly enhanced frequency selectivity, and consequently synchronisation advantages, over OFDM [9], [10].

Generally, filter bank based transceivers operate at a baseband level where well defined frequency bands are allocated to multiple users, or sub-channels. With a large amount of progress being made in the development of high-speed Analogue-to-Digital Converters (ADCs) and Digital-to-Analogue Converters (DACs) [11], the possibility of operating a filter bank transceiver up to RF is becoming an appealing possibility. Operating in this manner could yield the frequency agility and selectivity required of TVWS devices.

In the UK, the TVWS region is confined to a single block of 40 channels between 470 and 790MHz, with each channel having a bandwidth of 8MHz. The US TVWS channels, however, have 6MHz bandwidth and are split into four separate regions of spectrum as outlined in Table I [12]. There is therefore very little similarity between the requirements of a TVWS device configured for the UK spectrum when compared with one designed for the US. However, this paper will detail how a single TVWS device can be made to work in both the UK and US spectrum with a few simple reconfiguration steps.

The paper is organised as follows. Section II provides an overview of partial reconfiguration techniques for FPGAs, while Section III is dedicated to the proposed transceiver architecture. The configuration of the transceiver for the UK and US regions is discussed in Section IV, with the proposed Partial Reconfiguration setup covered in Section V. Simulations are presented in Section VI and, finally, conclusions are drawn in Section VII.

II. Partial Reconfiguration in Field-Programmable Gate Arrays (FPGAs)

Partial Reconfiguration (PR) is a dynamic reconfiguration technology which enables a FPGA device to be partially reconfigured on-the-fly; that is, a part (or multiple parts) of the FPGA can be reconfigured while the rest of the device continues to operate as normal. This technique lends itself well to the concept of software defined radio, enabling a single FPGA device to support a multitude of radio functionalities while sharing the same hardware resources [13]. This can be achieved by dynamically altering the functionality of the device by downloading partial bitstream files from external memory [14], [15].

The process of PR design involves designating regions of the FPGA as static or reconfigurable. The functionality of the reconfigurable regions can be altered dynamically without impact on the rest of the design. Each reconfigurable region can have multiple associated reconfigurable modules, which are operated with time multiplexing, i.e. only one of these modules is in use at any given time. In this study, partial reconfiguration will be employed to enable specific parts of the radio architecture to take on the functionalities required by the UK or US standards, as required.

III. System Approach

The proposed transceiver design aims to up- downconvert $K_c^{(i)}$ TVWS channels, where $K_c^{(i)}$ is the number of channels

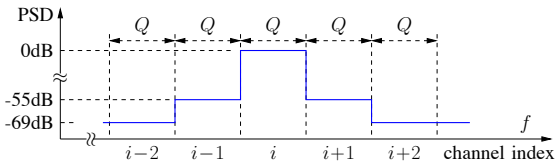

Fig. 1. Spectral mask defining permitted PSD levels in adjacent ($i \pm 1$) and next-adjacent 8MHz TVWS channels ($i \pm 2$) [1]. Q = {6,8}MHz according to configuration.

corresponding to the ith configuration as detailed in Table I. On the transmitter side, the upconverter must be capable of conforming to the regulator's imposed spectral mask requirements [1]. A Filter Bank MultiCarrier (FBMC) system will be used to allow the transceiver to provide adequate frequency selectivity to fulfil the imposed spectral requirements.

As the transceiver is to be implemented on a FPGA device, a number of considerations must be taken into account for the filter bank design. The first of these considerations is the upper limit to the sampling rate which can be realistically achieved. As current FPGA devices are unable to operate at RF sampling rates, external multiplexing and de-multiplexing must be performed on the input and output signals. This external processing introduces a further limitation to the number of external i/o streams which can interface with the FPGA.

The implementation of a FBMC system is most efficient in terms of both hardware and latency when constructed as a single filter bank. However, when taking into account the FPGA considerations discussed above, a single filter bank is unachievable. Therefore, a multi-stage transceiver design is adopted. Fig. 2 outlines the first two stages of the proposed transceiver design which links $K_c^{(i)}$ TVWS channels to an RF signal, with reconfigurable elements highlighted.

Taking the transmitter in the top part of Fig. 2, the baseband TVWS channels are sampled at a rate of f_b. In a second stage, an oversampled synthesis filter bank combines the $K_c^{(i)}$ baseband TVWS channels into a single synthesis signal. In the first stage, the synthesis signal is corrected by modulation with a complex exponential of normalised angular frequency Ω such that the channels will be correctly centred in the TVWS region after being filtered by a complex valued polyphase bandpass filter. The real valued part of the output forms the RF signal which is sampled at f_s.

The receiver is implemented using matching dual components to the transmitter, with the incoming RF signal being sampled at rate f_s. A complex bandpass filter creates an analytic signal which is corrected to DC by modulation prior to the $K_c^{(i)}$ TVWS channels being extracted by an oversampled filter bank. The filter bank is oversampled by a factor of two in order to ease further filtering and synchronisation of the individual TVWS channels.

IV. Transceiver Configuration

This section outlines the configuration of the TVWS transceiver in Fig. 2 with initial focus on the UK TVWS specifications. Reconfigurability of each element of the design will be highlighted, for flexible use in both UK and US markets.

TABLE I
TVWS Channels, corresponding frequencies and configurations for stage 1. [12]

Configuration i	Total Channels $K_c^{(i)}$	Region (US)	Channel Range	Frequencies (MHz)	Bandwidth B_i (MHz)
1 (UK-1)	40	-	21-60	470 - 790	320
2 (US-1)	12	1	2-4	54-72	162
		2	5-6	76-88	
		3	7-13	174-216	
3 (US-2)	38	4	14-51	470-698	228

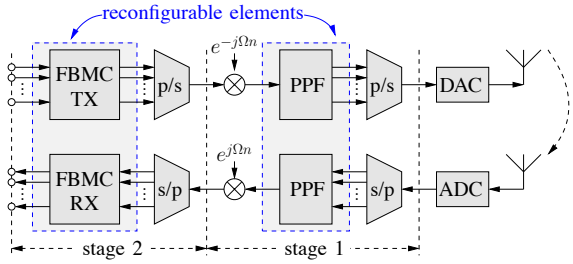

Fig. 2. Proposed reconfigurable TVWS filter bank transmitter (above) and receiver (below) with a polyphase filter (PFF) in stage 1 and a FBMC modulator in stage 2.

A. Stage 1

The first stage of the receiver isolates the TVWS bands from the $f_s = 1.92$GHz sampled RF signal. These isolated bands have a centre frequency that is equidistant from the upper and lower frequencies of the the particular TVWS band in question. These are used to create an analytic TVWS baseband signal that is aligned at DC. To extract the TVWS channels, firstly an analytic bandpass filter is used. This bandpass filter is centred at f_c and has bandlimitation which will allow decimation by a factor K_1.

With the reconfigurability of the device in mind, an initial downsampling factor should be chosen to enable not only UK TVWS channels, of 8MHz width, to be transmitted and received, but also US channels, of 6MHz width. With the chosen RF sampling frequency of $f_s = 1.92$GHz, an initial downsampling factor of $K_1 = 4$ will satisfy this condition ($\frac{1.92\text{GHz}}{4} = 480$MHz which is divisable by both 6MHz and 8MHz).

Aliasing is allowed in the transition band, permitting a transition bandwidth $B_{\mathrm{T},1}$,

$$B_{\mathrm{T},1} = \frac{1.92\text{GHz}}{K_1} - B_i \quad . \tag{1}$$

where B_i is defined in Table I. The required filter characteristic is shown in Fig. 3.

In order to align the TVWS bands so that they start at DC, a correction by the lower frequency f_b can be accomplished by selecting

$$\Omega = 2\pi \cdot f_b \cdot \frac{K_1}{f_s} \quad . \tag{2}$$

In the case of the UK and US-2 configurations, $f_b = 470$MHz. For US-1 configuration, $f_b = 54$MHz.

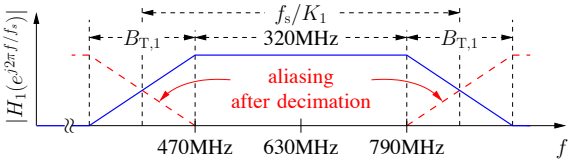

Fig. 3. Stage 1 (UK-1) filter characteristic with passband of 320MHz to capture the TVWS spectrum, and transition bandwidth $B_{T,1}$.

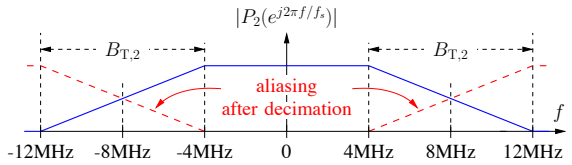

Fig. 4. Stage 2 (UK-1) filter characteristic with passband width of 8MHz and decimation to 16MHz sampling rate.

The implementation of the transmitter in stage 1 is a dual of the receiver, implemented in reverse order. A frequency shift by Ω is followed by upsampling in the form of an interpolating bandpass filter $H_1(e^{j\Omega})$. Here, the widened transition bands do not effect the output signal due to the tight spectral mask constraints that are imposed on the signal input to stage 1. The RF signal comprises of the real part of the analytic signal that is passed through an ADC sampling at RF rate.

B. Stage 2

With decimation at stage 1 of $K_1 = 4$ and $f_s = 1.92$GHz, stage 2 will extract $K_2 = 60$ 8MHz channels, or $K_2 = 80$ channels of 6MHz bandwidth. For the UK configuration, only the first 40 channels will be used and for the US-1 and US-2 configurations, only the first 12 and 38 will be used respectively. A modulated filter bank is an efficient approach here due to the uniform ordering of the channels. As previously mentioned, each channel will be oversampled by a factor of two in order to ease synchronisation in the baseband, and also to ease the filter characteristic, which is shown in Fig. 4. Similarly to stage 1, a maximum transition bandwidth $B_{T,2}$ is possible. It is assumed at this point that all TVWS channels have been perfectly bandlimited within the permitted channel width before being input to stage 2.

Here a form of DFT modulated filter bank is employed where, unlike the standard design, the analysis filter bank in the receiver employs a generalised IDFT and the synthesis bank in the transmitter a generalised DFT. This allows channels to be aligned from DC in ascending order.

C. Stage 3

The third stage represents baseband processing of individual TVWS channels, and has not been considered as part of this study. It contains the necessary band limitation and creates a Nyquist system between the transmitter and receiver, providing near-perfect reconstruction. Synchronisation is also handled in this stage.

A Nyquist(3) system is employed to create a simple test system, with the baseband signal sampled at a rate of (16/3)MHz. The filter characteristic of the root-Nyquist system employed in the transceiver is shown in Fig. 5. The combination of the

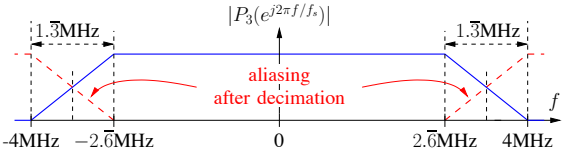

Fig. 5. Stage 3 (UK-1) root-Nyquist(3) filter characteristic with passband width of 5.3̄MHz and 16MHz sampling rate (for test purposes).

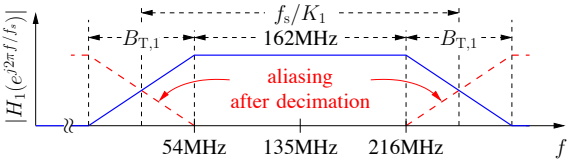

Fig. 6. Stage 1 (US-1) filter with passband width of 162MHz to capture lower portion TVWS spectrum, and transition bandwidth $B_{T,1}$

filters used in stages 2 and 3 must satisfy the spectral mask in Fig. 1.

V. Proposed Partial Reconfiguration Setup

The following section details the proposed PR system setup, focussing on the definition of Reconfigurable Partitions (RPs) and their associated Reconfigurable Modules (RMs). Furthermore, the problems associated with clock signal reconfiguration will be discussed.

A. Partial Reconfiguration Hierarchy

By definition, a Reconfigurable Partition (RP) is an area of an FPGA device to which PR is applied. Each RP has the ability for the logic to be swapped, thus changing the functionality, using PR while the remainder of the device continues its operation [13]. A Reconfigurable Module (RM) is the swappable logic that is associated with the RP. Multiple RMs can be associated with a single RP, but only one RM can be present in the RP at any given time [15]. PR provides the ability to reconfigure only the areas of the FPGA device which require it. This is advantageous as it yields significant savings in reconfiguration time over reconfiguring the entire FPGA device. The main reason for this being that when reconfiguring the entire device, the configuration time includes the intialisation time plus the configuration time [16]. With PR, however, this is not the case as the rest of the FPGA device continues to operate during the reconfiguration of the RP. A secondary factor is that the size of the partial bitstream will be smaller than a full bitstream, both in terms of physical hardware area and storage requirements, and thus requires less configuration time.

With reference to Fig 2, two reconfigurable elements are identified within the transceiver. On expansion of the system, each reconfigurable element contains two further RPs, one each for the transmitter and receiver side. In total, therefore, the transceiver design would contain four RPs. In terms of the associated modules, each RP would have three RMs - one for the UK configuration and one each for the two US configurations as defined in Tab. I.

With the various RPs and RMs defined in order to allow the transceiver to use PR, one problem remains - the different

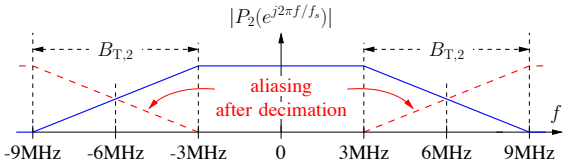

Fig. 7. Stage 2 (US-1,2) prototype filter with 6MHz passband width and decimation to 12MHz sampling rate.

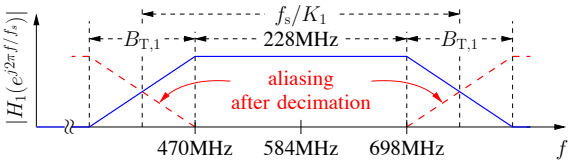

Fig. 8. Stage 1 (US-2) filter with passband width of 228MHz to capture upper portion TVWS spectrum, and transition bandwidth $B_{T,1}$.

configurations all require to be operated at different clock rates. The implementation of PR does not enable the clock frequency to be dynamically changed as the Digital Clock Manager (DCM) that is used to synthesise the clock must be implemented in static logic [13]. Therefore, PR alone is not sufficient for the implementation of the reconfigurable transceiver system. Fortunately a further reconfiguration technology, Dynamic Reconfigurable Port (DRP), can be used to overcome this problem. DRP allows the output frequency of the DCM to be reconfigured while the transceiver is in operation [16]. Thus, combining the PR and DRP techniques allows for the implementation of a transceiver which is capable of reconfiguring not only filter designs and architectures, but is also able to reconfigure to a number of different clocking frequencies despite being driven by a single oscillator.

Since devices operating in the TVWS spectrum will be required to consult a database of transmission channels for selection of a vacant channel for operation [12], an embedded processor can configure the device to transmit on a specific channel and also load the appropriate partial bitstream. The transceiver therefore has the ability to swap between configurations on-the-fly.

This proposed architecture has a number of benefits. By using PR, a number of RMs can access the same hardware resources in a single RP via time-sharing, thus increasing the efficiency of the FPGA device utilisation. Furthermore, through the use of DRP, the number of oscillators required by the design is reduced.

VI. Simulations and Results

This section presents some results of the filter design, detailing the PSDs of signals at various stages throughout the implementation with particular focus on adjacent channel leakage.

A. UK Filter Characteristics and PSDs

Fig 9 presents the magnitude responses for the three transceiver stages of the UK configuration as root Nyquist systems. It is clear that these responses satisfy the stopband edges and the attenuation by -69dB in the adjacent channel as imposed by the spectral mask in Fig. 1.

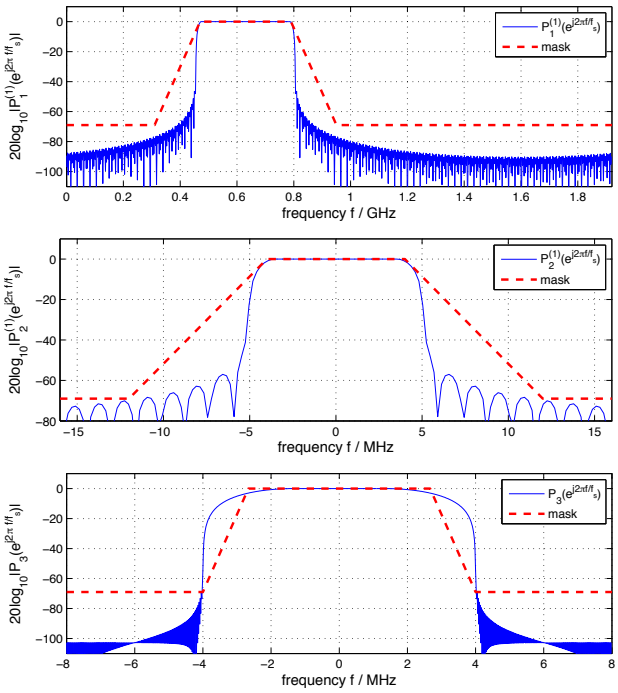

Fig. 9. Magnitude responses of (top) stage 1, (middle) 2, and (bottom) 3 prototype filters for UK configuration.

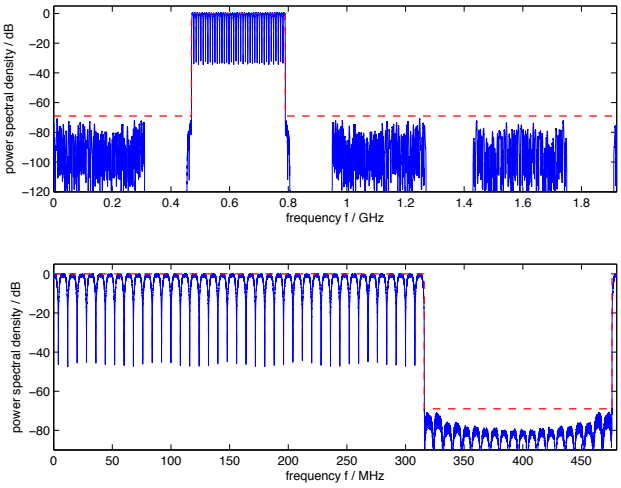

Fig. 10. Power spectral densities of stage 1 (top) and stage 2 (bottom) signals, with spectral masks indicated as dotted lines (UK).

The power spectral densities of simulated signals at each stage are shown in Fig. 10. Stage 1 occupies the full TVWS band from 470-790MHz, whereas stage 2 represents the downconverted TVWS band with $K_1 = 4$ and $K_2 = 60$ 8MHz channels, of which only the first 40 are occupied. The remaining 20 channels are vacant and display sufficiently low leakage.

B. US Filter Characteristics and PSDs

The magnitude responses of the prototype filters in stage 1 of each configuration for US TVWS are displayed in Fig. 11, showing that in each case the appropriate portion of the

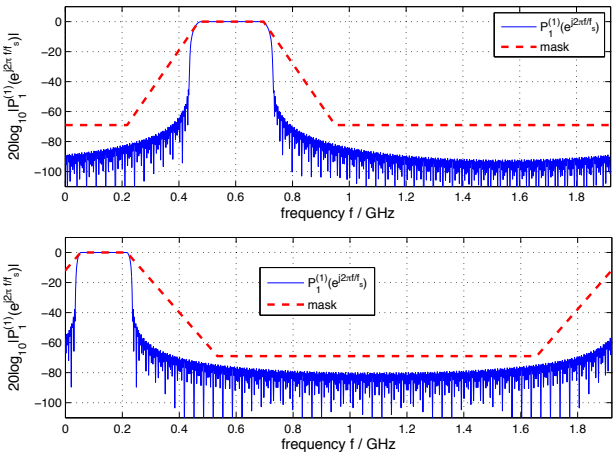

Fig. 11. Magnitude responses of stage 1 prototype filters for (top) US-1 configuration and (bottom) US-2 configuration.

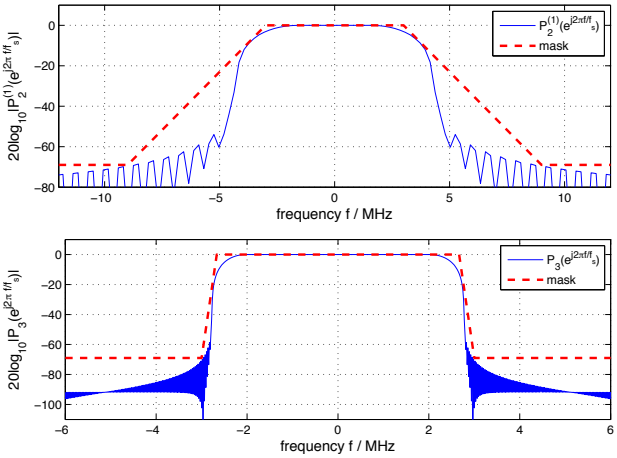

Fig. 12. Magnitude responses of stage 2 prototype filter (top) and stage 3 prototype filter (bottom) for US-1 and US-2 configurations.

US TVWS spectrum is extracted. Fig. 12 shows the filter response of the stage 2 and 3 prototype filters used in both configurations. All filter responses clearly indicate sufficient attenuation by -69dB in adjacent channels as imposed by the spectral mask.

The power spectral densities of simulated signals at each stage for configuration US-1 are shown in Fig. 13 and for US-2 in Fig. 14. It can be observed that for each configuration, stage 1 occupies the appropriate portion of the TVWS band. For $K_1 = 4$, stage 2 represents $K_2 = 80$ 6MHz channels, where only the first 12 and 38 are occupied for configurations US-1 and US-2 respectively. Once again, the low leakage in the remaining vacant channels satisfies the imposed requirements.

VII. Conclusion

A multi-stage FPGA based filter bank transceiver has been discussed which is capable of simultaneously up- and down-converting the entire UK TVWS region of 40 8MHz channels. Further discussion details how the technique of FPGA partial reconfiguration can be used to allow the transceiver system

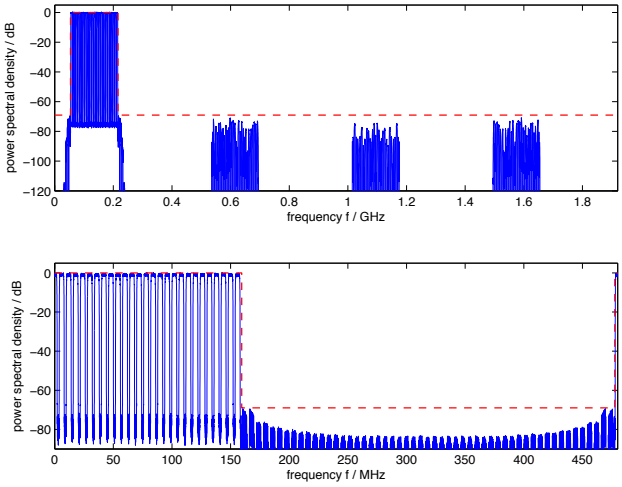

Fig. 13. Power spectral densities of stage 1 (top) and stage 2 (bottom) signals, with spectral masks indicated as dotted lines (US-1).

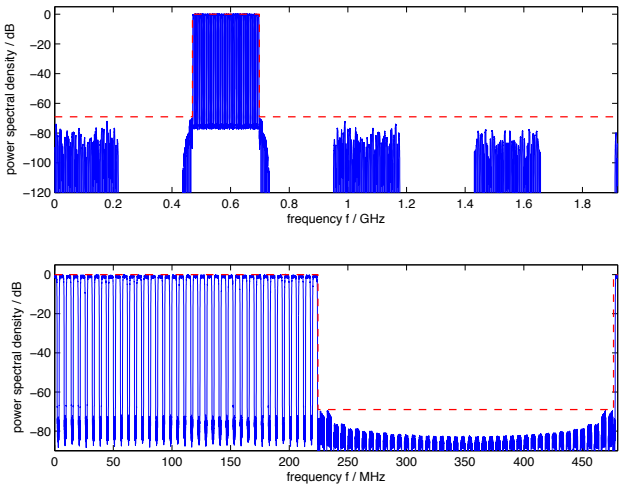

Fig. 14. Power spectral densities of stage 1 (top) and stage 2 (bottom) signals, with spectral masks indicated as dotted lines (US-2).

to be reconfigured for use in the US TVWS spectrum, and the consequent filter designs and reconfigurable sections are shown.

The various configurations and designs are motivated by a hypothetical ADC/DAC which is capable of operating at a sampling rate of 1.92GHz. The multi-stage approach was adopted in order to satisfy the input limitations and sampling rate restrictions of current FPGA devices.

The reconfiguration technologies required to efficiently implement the transceiver on a single FPGA device have been introduced and their usage in the system architecture discussed.

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