Demonstration of Sustained and Useful Converter Responses during Balanced and Unbalanced Faults in Microgrids

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***Abstract*-In large power grids where converter penetration is presently low and the network impedance is predominantly reactive, the required response from converters during faults is presently specified by phrases such as "maximum reactive output". However, in marine and aero power systems most faults are unbalanced, the network impedance is resistive, and converter penetration may be high. Therefore a balanced reactive fault current response to an unbalanced fault may lead to over-voltages or over/under frequency events. Instead, this paper presents a method of controlling the converter as a balanced voltage source behind a reactance, thereby emulating the fault response of a synchronous generator (SG) as closely as possible. In this mode there is a risk of converter destruction due to overcurrent. A new way of preventing destruction but still providing fault performance as close to a SG as possible is presented. Demonstrations are presented of simulations and laboratory testing at the 10kVA 400V scale, with balanced and unbalanced faults. Currents can be limited to about 1.5pu while still providing appropriate unbalanced fault response within a resistive network.**

INTRODUCTION

Within modern marine and aeronautical power networks, both drives and generators are increasingly being coupled via power-electronic interfaces. For drives, this allows the use of thrusters or propellers which can be positioned flexibly around the vessel or aircraft, and operated at different speeds. For generators, this allows different sizes and types of generators to be interfaced to the power system, each one operating at an independent rotational speed. Some power sources may consist of non-rotating equipment such as fuel cells, batteries, or super-capacitors etc.. Some electrical power sources may even use renewable energy devices such as photovoltaic panels, or energy-recovery systems such as thermo-electric heat recovery devices. These features have many benefits such as:

- Flexible siting of generators and propulsors.
- Flexible operation of generators to minimise fuel cost and wear/tear.
- Redundancy and post-fault reconfiguration.

While these systems have obvious benefits, a number of technical details need to be considered as the proportion of equipment interfaced through such power electronics increases. Amongst these issues are:

- Power system harmonics and harmonic filters [1].
- The "synthetic" inertia of the converters, how the converter software synthesises it, and where the energy flows to/from during dynamic events, and how [2].
- How the converters deal with unbalanced loads and voltages [3].
- The performance and robustness of the converters under fault conditions.

When addressing these issues, one of the main aims generally stated is to make the power-system facing converters emulate synchronous generators (SGs) as closely as possible. In this way, equal power sharing can be achieved via setting of appropriate droop slopes and by matching the synthetic inertias of converters with the actual inertias of directly-coupled SG units. If this could be achieved exactly, then, for example, a 1MW SG unit could be stood down and replaced with a 1MW converter-connected power source, but the response of the resulting power system to step load changes, non-linear loads, unbalanced loads, or faults, would be unchanged.

In practice, exact emulation of SG performance is difficult, and is still the subject of much research. Firstly, the converter contains no real inertia and this must be synthesised using software. For example [2] presented one approach to inertia emulation but there are several other approaches. Within land-based renewable power systems e.g. wind parks, there is much talk of requiring synthetic inertia provision but it is not clear where the energy will come from to synthesise large per-unit inertia ratings which can be sustained for anything more than a few tenths of seconds. Within a marine or aeronautical electrical power system, the energy store or transfer of torque also needs to be carefully accounted for.

Secondly, most converters (even so-called "voltage source converters" which use a DC bus capacitor rather than inductor) use inner current loops which are designed to source balanced sinusoidal currents. This is particularly true for land-based grid-connected converters which need to comply with standards such as IEEE 1547 [4]. Very few examples of significantly-sized network-connected converters in literature make reference to the provision of power to non-linear unbalanced loads, or sharing of power to such loads

with other converters or SG units. Proposed designs which do typically require high switching speeds, complex control algorithms, or high-bandwidth communication between converters which are closely coupled through low-impedance busses (typical within marine or aero power systems) [5].

Thirdly, the current capacity of converters is limited by the rating of the semiconductor devices and output filter inductors. Even short-term current overloads can lead to destruction if the output filter saturates and the semiconductors are exposed to multiple times their rated currents. So, while it may be possible to address synthetic inertia and non-linear unbalance power sharing issues using novel converter software designs, it will never be cost-effective to obtain the same magnitude of fault currents from converters as the 8-10x rating fault currents that SGs provide due to their transient reactances [6]. Generally, converter outputs are limited to about 2x the nominal values, otherwise semiconductor and filter components need to be excessively over-engineered. Therefore, a compromise must be made. The converter software needs to take deliberate action during faults, primarily to protect itself but also to provide as much fault current as possible to enable fault detection and isolation.

Fault Current Provision From Converters

For land-based grid-connected systems, the required fault performance is specified simply by wording such as "generate the maximum possible reactive current without exceeding the transient rating limit of the Power Park Module" [7] [8] [9]. The implication is for balanced reactive current outputs, even during unbalanced faults, and the compliance curves against voltage dips are only given as "% of nominal" values, giving no firm indication of unbalanced fault requirements.

Within a marine or aero power system, outputting maximum balanced reactive currents during a fault is inappropriate. The system cables (and faults) are predominantly resistive, and so active and not reactive power may need to be provided from the converter terminals. Trying to force reactive current into a resistive load (and vice versa) does not work and generally results in rapid frequency excursions leading to converter trips. For higher impedance balanced faults, and high rating converters, full output current might cause a balanced overvoltage event. For the most common unbalanced faults, maximum output current tends to over-volt the phases which are not faulted.

It is notable that a SG unit automatically achieves the "correct" load/fault response into any balanced or non-linear load/fault, since it behaves as a balanced set of voltage sources and not a set of current sources [6]. Thus, for any given load/fault scenario, the appropriate and expected currents flow naturally, based upon the network impedances at the time. While a converter is not capable of producing the same magnitude of fault currents as an equivalently-rated SG, if an converter is programmed to behave as closely to a voltage source as possible, instead of a current source, then it will tend to provide SG-like performance naturally, sharing unbalanced and non-linear loads, and, as far as possible, providing appropriate fault currents during all types of faults, without the risk of causing over-voltages.

A Method for Emulating Synchronous Generators

One implementation of SG emulation is given in [2], but in this paper a much simpler method is adopted. This is the "Voltage Drive" algorithm, initially presented in [3] as a means of offering improved AC power quality in weak grid-connected scenarios, but equally applicable to islanded and other power-sharing networks such as marine and aero. The control strategy is outlined in Fig. 1.

In this mode, the converter measures voltage at the midpoint of the "LCL" filter, where the capacitors are connected. The currents are also measured in the secondary inductor which faces the power network. A phased lock loop (PLL) tracks the voltages, and allows the controller to operate in the "*dq*" synchronous reference frame via the use of Park and inverse-Park transforms. The PLL provides a degree of "synthetic inertia" although the effect is complex and beyond the scope of this paper. The PLL also allows the converter to ride through faults or other dynamic events due to the action of the integral controllers within it, particularly if the PLL bandwidth is deliberately reduced during fault events when the voltage may be significantly depressed and the PLL may have only a very low or unbalanced voltage set to measure. Note that one advantage of measuring the voltages at the LCL midpoint is that even a bolted short at the converter terminals allows finite voltages to remain at the LCL midpoint due to the voltage divider formed by the primary and secondary filter inductances.

The converter is configured with target (nominal) frequency and voltage values, and also droop slopes against active and reactive power respectively. This leads to modified targets of frequency and voltage which change in real time according to the system load. The converter attempts to maintain the targets using PID control loops which control the angle and magnitude of the voltage synthesised at the switching bridge, which is termed E_{dq}^{p1}, since it is a drive voltage in the synchronous *dq* frame, containing a (p)ositive sequence component only at the (^{1}) fundamental. The primary coupling is to adjust the drive angle (relative to the PLL phase) to achieve the required frequency, and to adjust the drive magnitude (i.e. modulation index) to achieve the required voltage. However, the coupling relationship is in fact more subtle and complex if the filter component losses are fully accounted for.

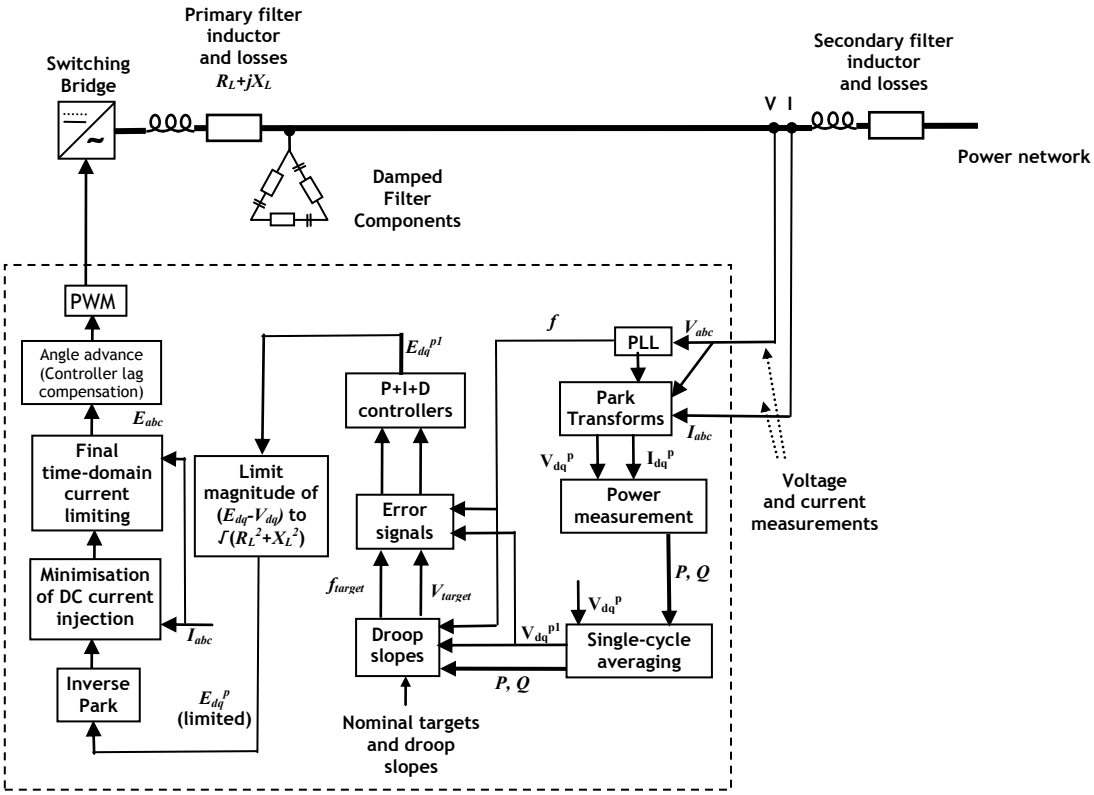

Fig. 1. Simplified control diagram for a converter in the proposed "Voltage Drive" mode, with drooped frequency and voltage targets.

This proposed mode requires only low-bandwidth control loops, and is therefore suitable for high-power converters in which a low switching frequency such as 2-4kHz is used. The effective controller delay is of the order of 1-2 switching cycles due to sample/processing delays and the length of the pulse-width modulation (PWM) waveform. This overall delay can be accounted for by adding an angle advance before the final park transformation and PWM generation.

The proposed method supports power-sharing of unbalanced and non-linear loads, since the software always tries to generate a balanced sinusoidal voltage set, coupled to the network via the filter inductors, and the controls are low bandwidth (lower than 50Hz). However, when a fault occurs there is the risk of overcurrent in the converter, since the control bandwidths are slow and will simply act to try and maintain frequency and voltage by holding the drive voltage E_{dq}^{p1} at a magnitude near 1.0 pu. Unless other action is taken, the per-unit fault currents will be approximately equal to the reciprocal of the total per-unit filter impedance, which will be of the order of 0.05 to 0.15, leading to 6-20pu currents and destruction of the converter.

To avoid this, 2 simple but effective limiting steps are added in a combined sequence [10]. Normally, the software implementing these steps is idle, and has no impact on operation. It is only triggered during the fault. The first limiting step is carried out on E_{dq}^{p1} in the synchronous *dq* frame as shown in Fig. 2. The theory of the limiting is simply that when expressed as simple balanced phasors and analysing the fundamental only, **V**=**ZI**, and therefore to limit **I** to a given magnitude, the per-unit voltage magnitude across the primary filter inductor R_L+jX_L must have a magnitude less than $I_{\max}\left|R_L + jX_L\right|$ where I_{max} is the per unit current limit. The actual limiting operates by clipping the actual drive voltage vector E_{dq}^{p} to make sure that it is within a range of $\alpha \cdot I_{\max}\left|R_L + jX_L\right|$ of the measured LCL midpoint voltage V_{dq}^{p} measured by the PLL. i.e.

$$\left|E_{dq}^{p} - V_{dq}^{p}\right| = \min\left(\alpha \cdot I_{\max}\sqrt{R^2 + X^2}, \left|E_{dq}^{p1} - V_{dq}^{p}\right|\right) \quad \textbf{(1)}$$

$$\angle\left(E_{dq}^{p} - V_{dq}^{p}\right) = \angle\left(E_{dq}^{p1} - V_{dq}^{p}\right) \quad \textbf{(2)}$$

where α is a factor close to 1, used to optimise the performance.

So, normally, the unadjusted voltage E_{dq}^{p1} is used to synthesise the PWM waveform, but during a fault the measured value of V_{dq}^{p} changes very quickly and the clipped drive voltage also changes very quickly, much more quickly than the usual controller bandwidth would allow. This allows low bandwidth controllers to be used, but still maintaining fast-reacting overcurrent protection.

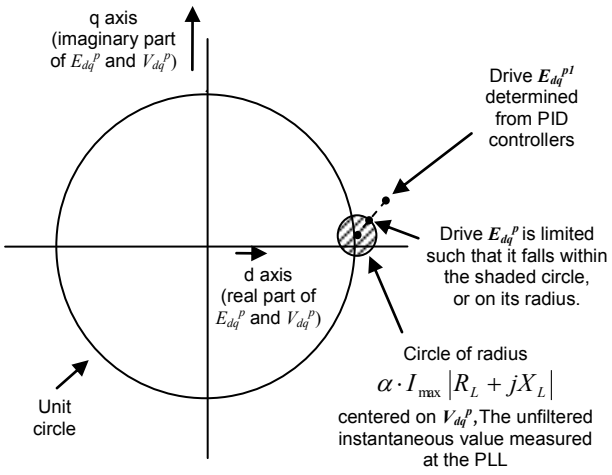

Fig. 2. Graphical represenation of limiting in the synchronous dq frame

This first limiting step is extremely effective at limiting currents during sustained balanced faults. However, during unbalanced faults. and during initial fault inception, there are both unbalanced and harmonic components present. Unbalanced components lead to a circular/elliptical oscillation of V_{dq}^{p} at twice the fundamental frequency [3]. This can be tracked by the *dq* frame reasonably well, but not perfectly due to the finite (low) switching frequency and resulting controller lag. Also, and more importantly, during initial fault inception there can be a significant DC (0th harmonic) component of voltage. This is captured in the *dq* frame as an circular/elliptical oscillation of V_{dq}^{p} at the fundamental, but unfortunately the resulting currents can still be very large since the filter impedance at DC is very low. Other harmonics are present in the fault voltage waveforms but these are of lesser concern since the filter impedance is proportionately higher.

To cope with the DC, unbalance and harmonic effects, a second step of limiting is applied. This is a more conventional limiting in the I_{ABC} domain. This simply checks the values of I_A, I_B and I_C in the secondary inductor to see if they are approaching the limits defined by I_{max}, and, if so, the final drive voltages E_{ABC} are adjusted by suitable amounts to hold the currents within limits. A useful step is also to then ensure zero sequence is removed from the drive voltages E_{ABC}, which balances the PWM waveform and minimises the risk of over-modulation at this time.

This second limiting step tends to cause distortion in the voltage and current waveforms, since it is a clipping in the time domain. If applied on its own, without the first limiting step in the *dq* frame, the distortion during even balanced faults is significant. However, when applied after the first limiting step, the second step only needs to make small adjustments, particularly within the first few milliseconds when DC effects are largest. The first limiting step in the *dq* frame does the bulk of the work, leaving the second step just to make small adjustments where current would otherwise have slightly exceeded the desired limits.

An additional step, which is required during normal operation but especially post-fault, is an additional set of low-bandwidth control loops which make tiny adjustments to the drive voltages E_{ABC} so that DC current injection/circulation is minimized at all times.

Results (Simulation)

The following results are taken from simulations of a 3-phase converter using such a control scheme. In this case the primary filter inductance was set to 0.15pu. The secondary filter inductance consisted of a star-delta transformer via which the simulated 3-phase (6 switch) converter was connected to a star-connected network.

Firstly, without either the 1st or 2nd limiting steps in place, Fig. 3 shows the response (Bridge currents at the IGBTs) to a balanced network fault at the converter terminals , with the resulting currents at up to 8pu, particularly at fault inception where DC components contribute. Adding the 1st step limiting in the *dq* domain (Fig. 4) limits the currents well, with I_{max} set to 1.25pu and α=1.25, but still leaves some initial instantaneous currents in excess of 1.5pu.

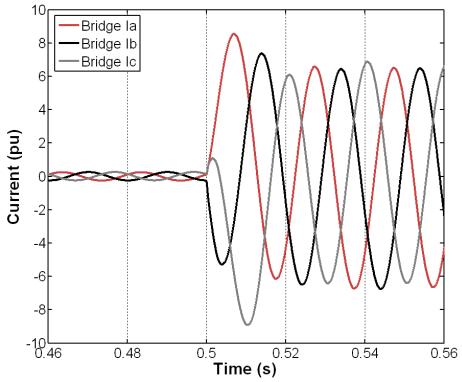

Fig. 3. Bridge Iabc (pu) in simulation for a balanced fault with no limiting applied

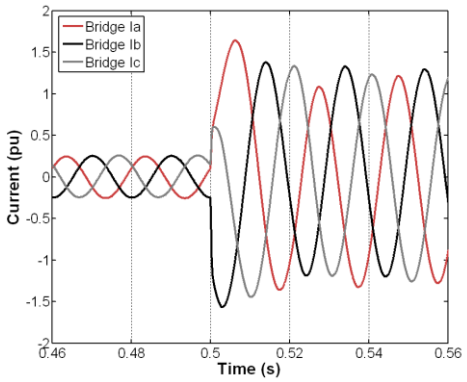

Fig. 4. Bridge Iabc (pu) in simulation for a balanced fault with only the 1st step *dq* limiting applied

Finally, further addition of the 2nd step limiting in the I_{ABC} domain to a target of I_{max}=1.25, leads to Fig. 5 where the currents are well controlled to a value close to the desired I_{max}, but without requiring waveforms with excessive clipping or distortion.

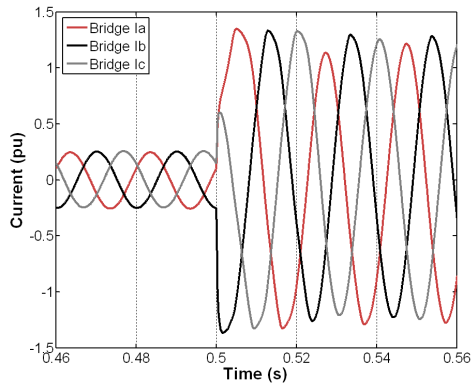

Fig. 5. Bridge Iabc (pu) in simulation for a balanced fault with both 1st step *dq* limiting and 2nd step limiting applied

If a single-phase to neutral fault is applied in the star-connected network, this results in a line-line fault within the converter due to the delta-star connection. The converter fault currents which result are shown in Fig. 6. Here, the current waveforms show a little more distortion as the converter software has to "work harder" to feed the unbalanced fault current, as the voltage and current trajectories in the synchronous *dq* reference frame are oscillating at twice the fundamental frequency.

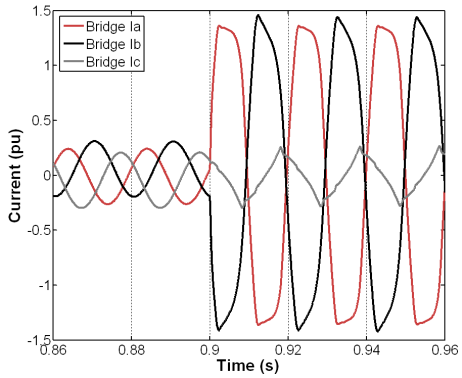

Fig. 6. Bridge Iabc (pu) in simulation for an unbalanced single phase to neutral fault in the power network (connected to the converter via a star-delta transformer) with both 1st step *dq* limiting and 2nd step limiting applied

RESULTS (HARDWARE)

The proposed method has also been tested using a physical converter, of nominal rating 10kVA, connected to a marine network test-bed at 400V RMS line-line, in a delta configuration. The converter was directly connected (transformerless) to the network via an LCL filter with a total inductive impedance of 0.072pu. The switching frequency was 4kHz, with a resulting frame time of 250μs. Power-sharing fault events were created by physically shorting lines at the terminals of the converter, which was initially only outputting a small output power. All 3 lines were shorted for balanced faults, or just lines 1 and 2 for unbalanced faults. To allow sustained faults to be studied with a minimum of danger, the impedance on the "distant" side of the fault (between the fault and the "upstream" network) was artificially increased to decrease the fault infeed at that side, which otherwise could have reached many kA.

First, a balanced fault for 140ms reveals the output (terminal) currents and (a LCL midpoint) voltages waveforms in Fig. 7 and Fig. 8. The currents are well controlled. There are very brief spikes visible at fault inception which are due to filter capacitor charge/discharge and these spikes do not appear in the primary inductor currents (at the IGBTs). It can be seen that the drive voltages are attempting to maintain a balanced voltage set at the IGBT bridge (Fig. 8), but the voltage magnitude which they can synthesise is limited by I_{max} and the filter impedance.

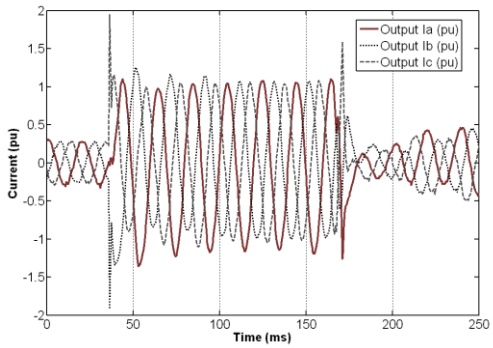

Fig. 7. Output Iabc (pu) in hardware for a balanced fault (L1 to L2 to L3)

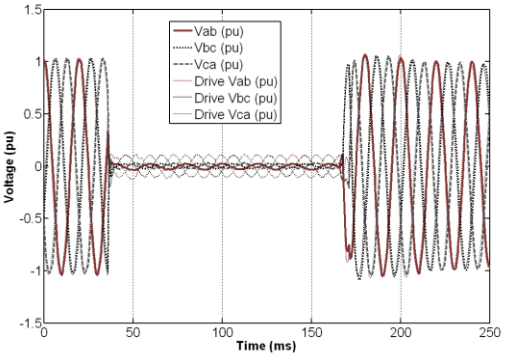

Fig. 8. Voltages at the LCL filter midpoint and drive voltages (pu) in hardware for a balanced fault (L1 to L2 to L3)

When a fault is applied only between line 1 and line 2 (L1 and L2), the fault currents and terminal voltages are highly unbalanced. Fig. 9 and Fig. 10 show the experimental data. In Fig. 9 the fault currents are slightly larger than 1.5pu at their instantaneous peaks. There is also some fault current flowing on L3, due to the actual network impedances, with the local network including devices such as a delta-delta and delta-star transformers feeding local loads. These provide coupling (which can be difficult or impossible to predict) between the phases due to zero-sequence effects and practical transformer behaviour. The voltages at the LCL midpoint, and the synthesised drive voltages, are show in Fig. 10. V_{ab} is small (the fault is between these phases), and so $V_{bc} \approx -V_{ca}$ since by

definition there can be no line-line zero-sequence voltage component in the 3-wire delta configuration.

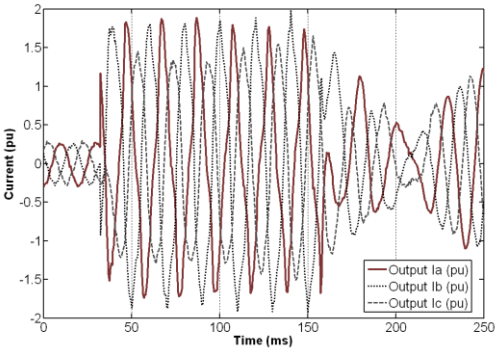

Fig. 9. Output Iabc (pu) in hardware for an unbalanced fault (L1 to L2)

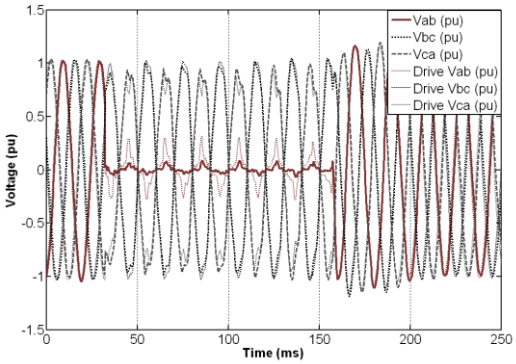

Fig. 10. Iabc (pu) in hardware for an unbalanced fault (L1 to L2)

CONCLUSIONS

The proposed control method is shown to be able to provide appropriate fault currents to balanced and unbalanced faults, emulating a SG fault performance as closely as possible, but without exceeding the current ratings of the converter. The converter is operated as a voltage source behind a reactance (its filter), which results in the appropriate currents flowing into whatever impedance the faulted or non-faulted network presents. This mode of operation also allows the converter to contribute to the sharing of unbalanced loads and non-linear loads, by sourcing unbalanced and non-sinusoidal currents when necessary [3]. The control method does not use an inner current loop. The current limiting portions of the software are only active during the fault and consist predominantly of a clipping action in the synchronous *dq* frame and additionally a small manipulation of modulated drive voltage waveforms to control DC and unbalanced fault currents.

In this paper, only the voltage and current traces from the fault events were presented. During the fault events, and during other dynamic events such as sudden load steps (rates of change of frequency) and voltage steps, overall converter performance is also heavily dependent upon its control loop setup and Phased Locked Loop (PLL) behaviour (if it has one). Many of the subtleties of this control remain to be fully understood and optimised. The converter response will depend heavily on, for example, any synthetic inertia which the converter is configured to have. During sustained fault events the configuration of the PLL (or synthetic inertia) is critical to avoid under/over frequency of the converter, or large resynchronising currents with other devices when the fault condition is removed. While holding converter frequency completely constant during a fault might be one solution, a better solution might allow converter frequency to rise during a fault in line with the expected behaviour of SG units, thereby minimising resynchronisation transients and torques.

ACKNOWLEDGMENT

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REFERENCES

[1] MAIB, "Report on the investigation of the catastrophic failure of a capacitor in the aft harmonic filter room on board RMS Queen Mary 2 while approaching Barcelona on 23 September 2010," Marine Accident Investigation Branch, REPORT NO 28/2011, 2010. Available: www.maib.gov.uk, accessed March 2012.

[2] Q. C. Zhong and G. Weiss, "Synchronverters: Inverters That Mimic Synchronous Generators," *IEEE Transactions on Industrial Electronics,* vol. 58, pp. 1259-1267, Apr 2011.

[3] A. J. Roscoe, S. J. Finney, and G. M. Burt, "Tradeoffs between AC power quality and DC bus ripple for 3-phase 3-wire inverter-connected devices within microgrids," *IEEE Transactions on Power Electronics,* vol. 26, pp. 674-688, 2011.

[4] IEEE, "IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems," IEEE 1547-2003, 2003.

[5] K. H. Ahmed, A. M. Massoud, S. J. Finney, and B. W. Williams, "Autonomous adaptive sensorless controller of inverter-based islanded-distributed generation system," *IET Power Electronics,* vol. 2, pp. 256-266, May 2009.

[6] P. C. Krause, O. Wasynczuk, and S. D. Sudhoff, "Analysis of electric machinery and drive systems," 2nd ed. chapter 5: New York : IEEE Press, 2002, pp. 229-232.

[7] National Grid, "The grid code," Issue 4 Revision 6, 2011. Available: http://www.nationalgrid.com, accessed May 2011.

[8] National Grid, "Guidance Notes for Power Park Developers," Issue 2, 2008. Available: www.nationalgrid.com, accessed March 2012.

[9] Eon-Netz, "Requirements for Offshore Grid Connections in the E.ON Netz Network," Updated: 1. April 2008, 2008. Available: http://www.eon-netz.com, accessed.

[10] A. J. Roscoe and S. J. Finney, "Method of controlling an inverter and a controller for controlling an inverter," GB patent application GB1114868.1, 2011.