Demonstration of a 1024-Channel Time Slot Selector for Ultrafast OTDM Networks

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Summary

OTDM networks can offer superior performance compared to other multiplexing methods where high speed switching is required over a large number of channels. To encode data on a desired channel, a delay line which is rapidly tunable across a large number of channels is required. Recently, a single transmitter generating 206 WDM channels has been reported[1] . In the paper, we demonstrate a tunable delay line which is able to access 1064 50-MHz channels with reconfiguration time of 20ns for a 50 Gb/s OTDM network. To our knowledge, this is the largest number of rapidly tuned to date, thus demonstrating that OTDM networks have potential of large dimensionality.

The device consists of multiple stage feed-forward delay line structure, one input and one output modulator (see Fig.1). Because the structure uses passive delays rather than 2x2 switches, it has lower insertion loss and complexity than the previously proposed delay line[2] . Each delay stage is a Mach-Zehnder lattice with differential time delay of T-τ, 2(T-τ), 4(T-τ),...(2^{k-1})(T-τ) between upper and lower path, where *T* is the incoming clock period and τ is the outgoing bit period. At the speed of the incoming clock rate, the input and output modulators are controlled by the gating functions, G_{in} and G_{out}, to set the state of the delay line. The total number of the accessible time slots, N, is related to the number of the stages, *k*, by $N=2^k\ 2^k$. For example, instead of 10 stages, only 5 stages are requires to generate 1024 channels in the delay line.

Figure 2 (a)-(d) show the timing diagram of the device. For simplicity, only the case of k=2 is presented. Each clock pulse (S_{in}) is split, time delayed, and combined to generate the 4-bit groups after the delay structure(Fig.2(b)). Groups of four pulses with interval of τ are generated consecutively at every T as shown in (c). This will repeat for 2^k=4 times to generate a 16-bit TDM frame (i.e., $N=2^2\ 2^2$). To select a designated time slot in the 16-bit TDM frame, a gating control provided by the E/O modulators is implemented at the input and output(Fig.2(a),(d)). From Fig.2, for a *k*-stage structure, the reconfiguration time is $2^k T$, where T^{-1} is the repetition rate of the input optical clock signal.

In the demonstration, 5-stage delay line was built. The differential fiber pair in each lattice was carefully adjusted using a permanent fiber stretching technique and monitored by an interferometric length measurement to achieve the precise timing with accuracy of 1ps [3]. 1.6 GHz optical clock was generated from a mode-locked Nd:YLF laser at 1.3μm (T=625 ps). Two $LiNbO_3$ modulators were employed to provide the gating controls at 1.6GHz. The overall loss of the device is about 24dB. Fig3(a) shows the oscilloscope trace of the output optical pulses that are tuned to different time slots. To demonstrate the fine tuning to the adjacent time slots spaced 20 ps apart, the single bit selected by the

input modulator from the 32-bit input clock was scanned consecutively from the 1st to the last bit. Fig.3(b) shows the measured output time delays from time slot #289 to #416, tuning across 127 time slots. The average reconfiguration time of the delay line is ~20ns.

References

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3. K.L Deng, K.I. Kang, I. Glesk and P.R. Prucnal, *CLEO*, Baltimore, MD, 1997, paper CThP6.

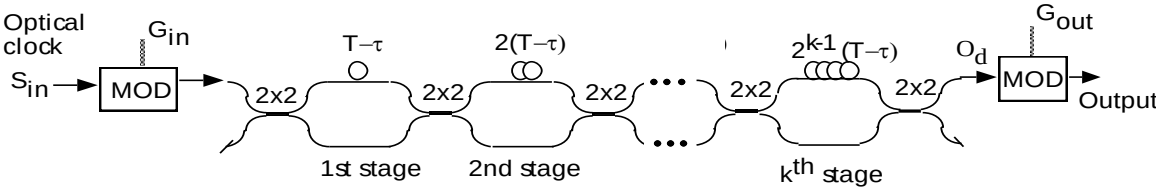

Fig.1 schematics of the device.

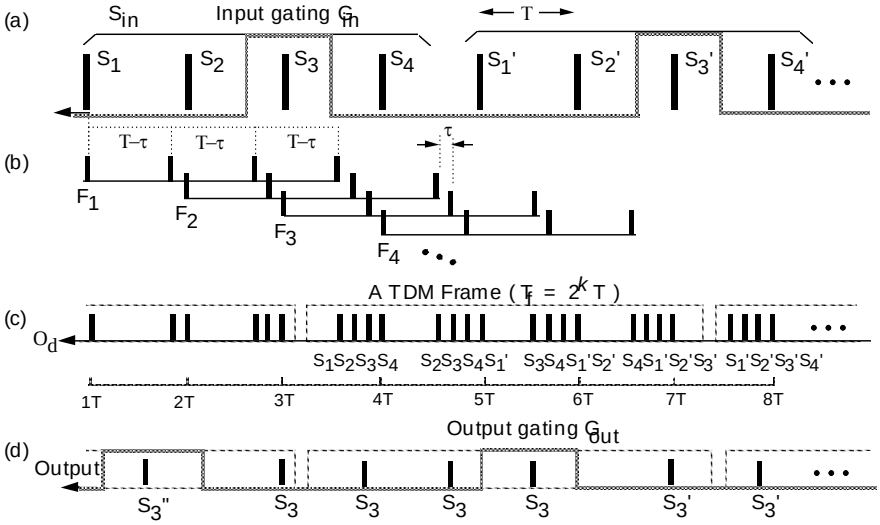

Fig.2 Timing diagram of the device. (a) the input clock (b) pulses after splitting in the delay line (c) the output after the lattice structure and (d) the output after the end modulator.

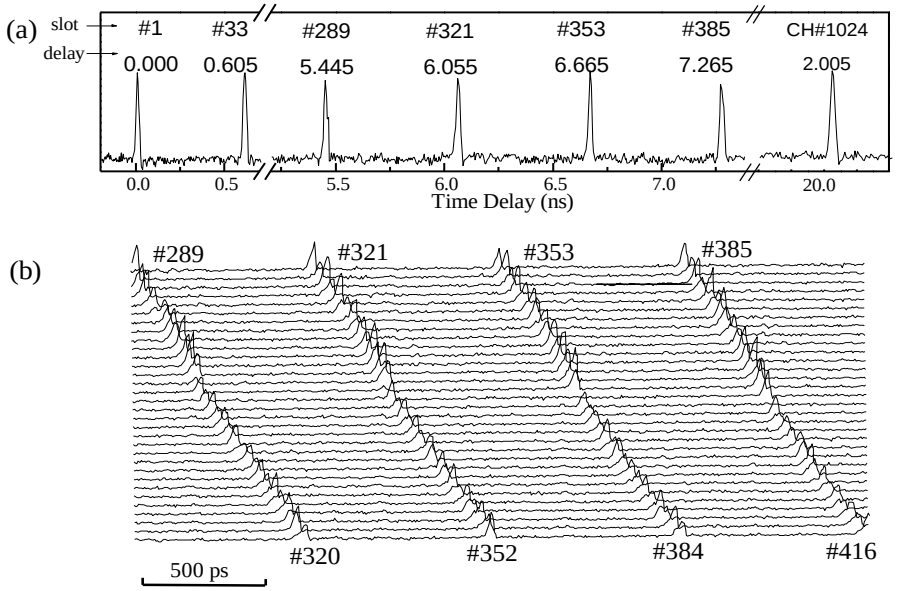

Fig. 3 Detected optical pulses with different time delays by a 32 GHz detector.