This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2336628, IEEE Transactions on Industrial Electronics

Power Conversion and Signal Transmission Integration Method Based on Dual Modulation of DC-DC Converters

Jiande Wu, *Member*, *IEEE*, Jin Du, *Student Member*, *IEEE*, Zhengyu Lin, *Senior Member*, *IEEE*, Yihua Hu, *Member*, *IEEE*, Chongwen Zhao, *Student Member* and Xiangning He, *Fellow*, *IEEE*

***Abstract*—For the development of communication systems such as Internet of Things, integrating communication with power supplies is an attractive solution to reduce supply cost. This paper presents a novel method of power/signal Dual Modulation (PSDM), by which signal transmission is integrated with power conversion. This method takes advantage of the intrinsic ripple initiated in switch mode power supplies as signal carriers, by which a cost-effective communications can be realized. The principles of PSDM are discussed and two basic dual modulation methods (specifically PWM/FSK and PWM/PSK) are concluded. The key points of designing a PWM/FSK system, including topology selection, carrier shape and carrier frequency are discussed to provide theoretical guidelines. A practical signal modulation-demodulation method is given and a prototype system provides experimental results to verify the effectiveness of the proposed solution.**

***Index Terms*— Power electronics, power line communication, power/signal dual modulation, pulse width modulation, distributed power system.**

I. INTRODUCTION

In new concepts such as the Internet of Things [1-3] and the Industrial Internet [4-5], machine-to-machine communication is the backbone of future industrial and civil electrical systems, consequently is receiving extensive attention. A large number of smart ‘things’ or ‘objects’ including facilities, equipment, devices and sensors tend to be connected to future electrical systems, and the big data produced by them is transmitted, stored and analyzed [6]. This brings challenges to make these electrical systems more intelligent and reliable.

Manuscript received January 27, 2014; revised April 24, 2014; accepted June 13, 2014.

This work is sponsored by the National Nature Science Foundation of China (61174157) and (51361130150).

J. Wu, J. Du, C. Zhao, and X. He are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: eewjd@zju.edu.cn; eedujin@zju.edu.cn; zcwxp@yahoo.com.cn; hxn@zju.edu.cn).

Z. Lin is with the Electrical, Electronic and Power Engineering of the Aston University, Birmingham, U.K. (e-mail: z.lin@ieee.org).

Y. Hu is with the Department of Electronic & Electrical Engineering, University of Strathclyde, Glasgow, UK. (e-mail: Yihua.hu@strath.ac.uk)

In most of traditional Distributed Control Systems (DCS), communication circuitry and power supply circuit are separately designed, so two independent circuits are needed. For example, in distributed power supply systems, additional communication circuits are added to receive control instructions from a supervisor controller or to exchange data between power converters [7-10]. On the other hand, for communication nodes in classic field bus systems, such as RS-485 or CAN, dedicated power converters are required to provide a stable power supply [11-12].

To simplify the wire connection of the system, two techniques are adopted [13-27]. The first technique is wireless communication, which has been widely used and increasingly accepted for industrial control systems [13-15]. However, due to the lack of physical protection, the security and reliability of wireless networks are often doubted, and other methods have been proposed for protection [16-17]. On the other hand, for most industrial systems, the nodes of wireless networks must be powered, so they inevitably connect with the power supply by wires. The second technique which simplifies connectivity is Power Line Communication (PLC), which originates from the so called second industrial revolution [18-20]. The idea of transmitting a signal on a battery powered cable was used in the London–Liverpool telegraph system, which was the earliest record of integrating the signal transmission through power cables [18]. Since the 1920’s, the invention of carrier frequency transmission (CTS) and ripple carrier signaling (RCS) techniques has made PLC an option for remote load control. By the late twentieth century, with the development of integrated circuits and the Internet, considerable progress has been made in modulation methods and its application scope [19]. Nowadays, PLC techniques cover both the high voltage transmission networks and medium/low voltage distribution networks, which can supply services such as voice transmission, internet access, remote meter reading and load control, over the power cable. The PLC channel model has been comprehensively investigated [20-21], with numerous applications reported [22-27]. This technique has proved a reliable method for communication.

However, both wireless communication and PLC require independent circuits to amplify the communication signal. For PLC, extra inductive or capacitive coupling units are required to embed the data signal into the power line, which increases system costs and volume.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2336628, IEEE Transactions on Industrial Electronics

In [28-29], the authors present a novel method that realizes power line communication between DC-DC converters which share a common input DC bus. Because the communication signal is inherently generated by the pulse width modulation of DC-DC converters, there is no need for an additional power amplifier to inject the signal on to the DC bus. This confirms the possibility of integrating communications into power conversion. However, these researchers mainly focus on signal processing, and the intrinsic relationships between the power electronic circuit and the communication model are not investigated.

This paper presents a power/signal dual modulation (PSDM) method to integrate data transmission with power conversion. The communication model and the methods of modulation/demodulation are analyzed in detail. The proposed technique of PSDM embeds a communication system into a power supply system, and is a cost-effective way to realize local communications for some power systems.

This paper is organized as follows. The PSDM principle is presented and analyzed in Section II. The applicable conditions, including topology choices and modulation methods are discussed in Section III. Modulation and demodulation methods are shown in Section IV. Prototype design and experimental verification are shown in Section V. Finally, conclusions are given in Section VI.

II. Principle of Power/Signal Dual Modulation

In power electronics, power converters are constructed with semiconductor switches and passive elements such as inductors and capacitors. Pulse width modulation (PWM) is the most popular strategy employed in the control of power converters. For the typical PWM waveform shown in Fig.1, the Fourier coefficients are

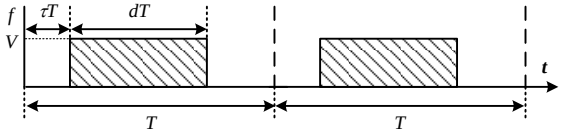


Fig.1 A typical PWM waveform.

$$f(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + \sum_{n=1}^{\infty} b_n \sin(n\omega t) \quad (1)$$

$$a_0 = dV \quad (2)$$

$$a_n = \frac{2V}{n\pi}\sin(nd\pi)\cos(2n\tau\pi + nd\pi) \quad (3)$$

$$b_n = -\frac{2V}{n\pi}\sin(nd\pi)\sin(2n\tau\pi + nd\pi) \quad (4)$$

$$c_n = \sqrt{a_n^2 + b_n^2} = \frac{2V}{n\pi}\left|\sin(nd\pi)\right| \quad (5)$$

where ω is the angular frequency of the waveform, d is the duty ratio associated with period T, τ is the delay time ratio of the pulse, which corresponding to the angular component of the harmonics. For conventional pulse width modulated circuits, the duty cycle d of each period is controlled to achieve a given average voltage which corresponding to the DC component of equation (1). Although being filtered, the high frequency harmonic components, with initial amplitude represented by (5), still exist at the input and output ports.

For a PWM system there are three freedoms that can be manipulated. Except the duty cycle d used by PWM, the frequency f and phase τ can be modulated to carry information, which correspond to the Frequency-Shift Keying (FSK) and Phase-Shift Keying (PSK) modulation in signal communications. So that PWM/FSK or PWM/PSK dual modulation can be employed to simultaneously realize power conversion and signal transmission, which is also termed power/signal dual modulation (PSDM).

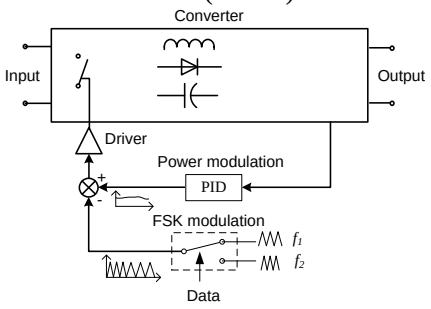


Fig.2 Block diagram of PWM/FSK dual modulation.

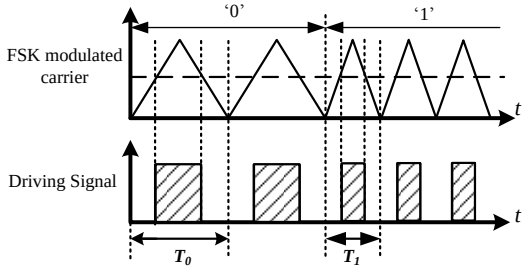
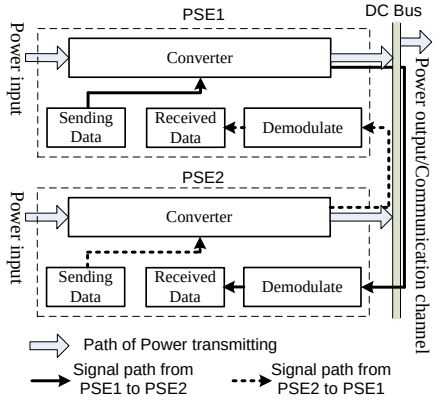


Fig.3 Drive signal of PWM/FSK dual modulation.

This paper focuses on PWM/FSK modulation and does not pursue PWM/PSK. Fig.2 shows the block diagram of a PWM/FSK dual modulated system. Different from conventional PWM, the carrier of the PSDM system is a FSK regulated PWM signal. A PWM/FSK modulated waveform is shown in Fig.3, where the circuit operates at frequency f_0 while sending data '0', and frequency f_1 while sending data '1'. The ripples in the input and output port waveforms carry information that has been modulated, on which a communication system depends.

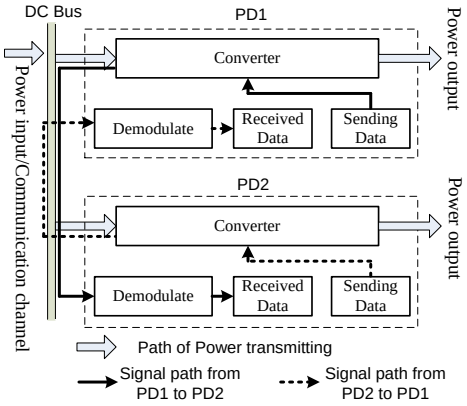
III. Applicable Condition and Communication Modeling

A. Structure of the PSDM system



(a) Load splitting structure of a PSDM system.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2336628, IEEE Transactions on Industrial Electronics



(b)Source splitting structure of a PSDM system.

Fig. 4 Two basic structures of a PSDM system.

The basic structure of conventional distributed power systems includes paralleling, cascading, load splitting, source splitting and stacking [30], which are also available for power/signal dual modulation system. In this paper, we define two fundamental devices: Power Sourcing Equipment (PSE) and a Powered Device (PD). PSE is a converter that communicates at the output while PD is a converter that communicates at the input.

The structure of load splitting is shown in Fig.4(a) while source splitting is shown in Fig.4(b). The difference between these two structures is the channel of communication, source splitting lies in the input while load splitting lies in the output.

B. Topology analysis for PSDM

Theoretically, all switching mode DC-DC converters can create additional high frequency voltage signals at their input or output, which could be used as a signal carrier. The additional voltage signal in the converter port includes two components, switching noise and switching ripple. Switching noise is sensitive to circuit design and the placement of switching components, so is difficult to utilize. Switching ripple is the voltage generated by converter ripple current, and is stable when the circuit component values are determined. The voltage ripple equals the product of current ripple and port equivalent impedance.

For basic dc-dc topologies such as buck and boost converters, it is difficult to predict the current ripple amplitude if the circuit operates in a discontinuous conductive mode (DCM), because the current ripple is sensitive to the load. So in this paper, all analysis is based on synchronous rectification (bidirectional current flow) to prevent DCM.

To achieve reliable communications, the carrier should be stable in magnitude, but for some power electronic topologies, the ripple is vulnerable to the variation of input voltage and output load. Therefore, the applicable operating conditions of each dc-dc topology should be assessed.

In a buck converter (Fig.5), the input current is pulsative (always discontinuous) and its amplitude is determined by the load, which means that the signal carrier is unstable so the buck converter is unsuitable for a PSDM-PD device. However, the output current of the buck converter is continuous and the ripple amplitude ($\Delta i=U_o(1-d)T_s/L$) is load independent. The basic harmonic amplitude of the output current ripple is

$$I_1=\frac{U_0T_s}{\pi^2 dL}\left|\sin(d\pi)\right|=\frac{U_0T_s}{\pi L}\left|Sa(d\pi)\right|=I_{1\max}\left|Sa(d\pi)\right| \quad (6)$$

where U_0 is the output voltage, T_s is the period, L is inductance.

For a voltage regulated buck converter, assuming the input voltage varied from $1.3U_0$ to $3U_0$, the duty cycle d changes from 0.33 to 0.77 while I_1 varies from $0.83I_{1max}$ to $0.27I_{1max}$, which is acceptable for signal communication.

From this analysis, it can be concluded that the buck converter is suitable for PSE, but not for PD.

Similarly, the input current of boost converter is continuous, and the ripple magnitude ($\Delta i=U_ddT_s/L$) is independent of load, while its base frequency amplitude is

$$I_1=\frac{U_0T_s}{\pi^2 L}\left|\sin(d\pi)\right|=I_{1\max}\left|\sin(d\pi)\right| \quad (7)$$

For a voltage regulated boost converter if d varies from 0.3 to 0.7, the output ripple I_1 changes from $0.81I_{1max}$ to I_{1max}. However, the output current of a boost converter is pulsative, that is discontinuous. Therefore the boost converter is suitable for PD, but not PSE.

The discussion in following section is based on the boost converter, which operates as a PD.

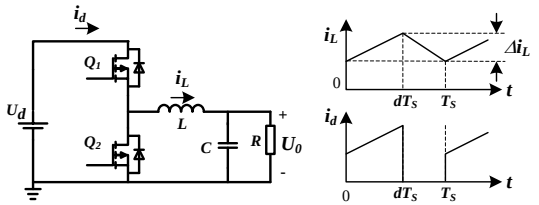


Fig.5 Buck converter and its current ripple.

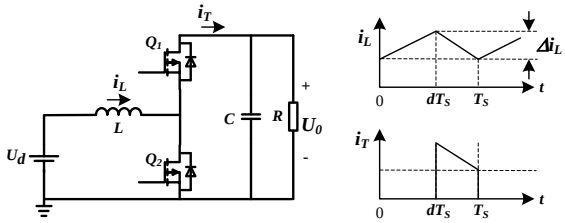


Fig.6 Boost converter and its current ripple.

Extending the analysis to other dc-dc converter topologies, the applicable suitability conditions (continuous port current) can be obtained, as summarized in Table. I.

TABLE . I
APPLICABILITY OF TOPOLOGIES

Converter topology	PD	PSE
Buck	Unsuitable	Suitable
Boost	Suitable	Unsuitable
Buck-Boost	Unsuitable	Unsuitable
Cuk	Suitable	Suitable
Sepic	Suitable	Unsuitable
Zeta	Unsuitable	Suitable

C. Shape of the modulated carrier

In a power/signal dual modulated converter, although power conversion and signal modulation are realized by a unified circuit, the control process of these two functions should be decoupled, which means the signal modulation should not affect the process of power conversion (and vice versa).

Assume that a boost converter operates in a PWM/FSK dual modulation mode, sawtooth wave is employed as carrier (giving single end modulation), as shown in Fig 7(a). Before

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2336628, IEEE Transactions on Industrial Electronics

the switching frequency shifts from f_1 to f_2, the average current is i_{AV1}, and the peak to peak current ripple is i_{L1}, then the current at the frequency shifting point is

$$i_L(t_s) = i_{AV1} + \frac{1}{2}\Delta i_{L1} = i_{AV1} + \frac{dU_d}{2Lf_1} \tag{8}$$

where U_d is the converter input voltage.

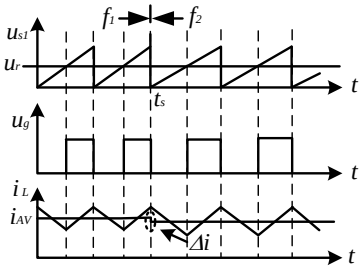
After the switching frequency shifts to f_2, assuming the duty cycle remains the same, the peak to peak current ripple is $\Delta i_{L2} = \frac{dU_d}{Lf_2}$, so the average current is

$$i_{AV2} = i_L(t_s) - \frac{1}{2}\Delta i_{L2} = i_{AV1} + \frac{dU_d}{2L}\left(\frac{1}{f_1} - \frac{1}{f_2}\right) \tag{9}$$

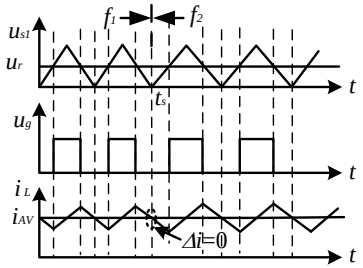
The average current difference before and after frequency shifting is

$$\Delta i_{AV} = i_{AV2} - i_{AV1} = \frac{dU_d}{2L}\left(\frac{1}{f_1} - \frac{1}{f_2}\right) \tag{10}$$

Because the average output current in one switching cycle is $i_{T\langle AV\rangle} = (1-d)i_{AV}$, the frequency shifting will produce a current perturbation even if the duty cycle remains constant, as shown in Fig.7(a). Therefore, embedding FSK modulation with a sawtooth carrier will introduce additional interference, which should be avoided in the design of the PSDM system.



(a) Sawtooth carrier



(b) Triangle carrier

Fig.7 Waveformsof the Boost circuit employing different carrier.

In Fig.7(b), a triangle wave is employed as a carrier (producing double edge modulation). The switching frequency shifts from f_1 to f_2 to modulate the intended signal. When the switching frequency is f_1, the average current is i_{AV1}, the peak to peak current ripple is i_{L1}. After the switching frequency shifts to f_2, the peak to peak current ripple is $\Delta i_{L2} = dU_d / Lf_2$, the average output current in one switching cycle remains the same, as shown in Fig.7(b).

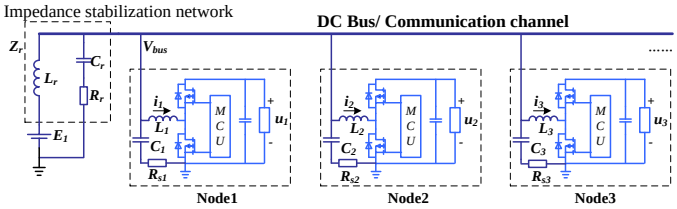
According to this analysis, it is concluded that a triangle wave is a better carrier option.

D. Communication model

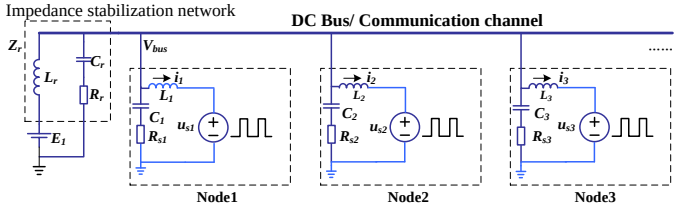
Take boost circuit as an example, Fig.8(a) shows a system composed of three nodes. V_{bus} is a common bus which is not only for powering the node but also for data communication. E_1 is a voltage source which supplies power to V_{bus} via an impedance stabilization network Z_r, which is comprised of a LCR network. The function of the inductor L_r in the network is to block the interference and impedance from the voltage source E_1, where L_r complies with

$$2\pi fL_r \gg R_r + 1/2\pi fC_r \tag{11}$$

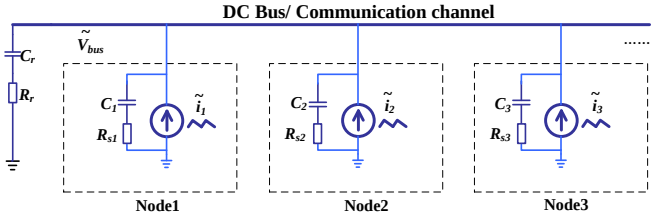
where f is the switching frequency. The capacitor C_r in the network is used to stabilize the bus, resistor R_r is the equivalent series resistance (ESR) of C_r.



(a) System structure.



(b) Replace boost circuits by pulse voltage sources.



(c) Simplified model for communication.

Fig.8 Communication model of a boost-based system.

The equivalent series resistance of a boost converter input capacitor, represented by $R_{s1\sim3}$, cannot generally be ignored. In steady state, the switch and output capacitor of the boost circuit is equivalent to a pulse voltage source from the point of view of signal communication (Fig.8 (b)).

Ignoring the dc component, the pulse voltage source and the inductor can be replaced by a triangle current source, so the diagram of the communication system is simplified to Fig.8(c). Without considering transmission line resistance, when n nodes are on the bus, the magnitude of the ripple voltage on V_{bus} is

$$\tilde{V}_{bus}(j\omega) = \frac{\sum_{k=1}^{n} \tilde{I}_k(j\omega)}{\frac{j\omega C_r}{1+j\omega R_r C_r} + \sum_{k=1}^{n} \frac{j\omega C_k}{1+j\omega R_{sk} C_k}} \tag{12}$$

When several nodes are connected to the bus, the waveform on the bus is the linear synthesis of the ripple produced by each node.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2336628, IEEE Transactions on Industrial Electronics

IV. MODULATION AND DEMODULATION METHOD

All the nodes in a PSDM system produce noise signals if they do not send a data signal, which is different from traditional PLC techniques. Assume that the data carrier and noise are deployed in the same spectrum of the channel, according to the Shannon theory of channel capacity, the maximum communication rate C which a system can be realized is determined by

$$C = B\log_2(1+SNR) \tag{13}$$

where B is the communication channel bandwidth and SNR is the signal to noise ratio. In a PSDM system of n nodes, assuming one node is sending and the others are waiting, the amplitude of either the signal or noise is equal, so the channel capacity of the bus can be express as

$$C = B\log_2(1+SNR) = B\log_2(1+\frac{1}{n-1}) \approx \frac{1.44B}{n} \tag{14}$$

Equation (14) shows that the communication rate decreases as the number of nodes increases, on the condition any signal or noise is filtered without any discrimination. However, the equation (14) restriction can be overcome if a dedicate filter removes the noise frequency component.

In a binary frequency shift keying (BFSK) based PSDM system, two strategies can be utilized to transmit the data signal. The first is a three-carrier strategy: a carrier of frequency f_{nom} is adopted when a node is waiting for communication, carrier f_0 is applied as sending signal '0' and carrier f_1 is applied as sending signal '1', such that carriers shift between three frequencies. The second is a two-carrier strategy: carrier f_{nom} is adopted when waiting for sending data or sending signal '1', carrier f_0 is applied as sending signal '0'. In this strategy, the carriers shift between two frequencies.

For a PSDM system, the carrier frequencies f_0 and f_1 should be selected as close as possible to f_{nom} to avoid adverse converter effects, such as stability and filter designing problems. However, the closer the frequencies, the more difficult to differentiate them.

Assume that N nodes are on the bus and only one node is transmitting signal '0', the base frequency of the bus ripple is

$$s(t) = A_1\cos(2\pi f_{nom}t+\varphi_1) + A_0\cos(2\pi f_0 t+\varphi_0) \tag{15}$$

where A_1 is the noise signal amplitude and A_0 is the amplitude of data signal '0'. A_1 is the synthesis of (N-1) waiting nodes and the value is variable because the carrier phase in every node is different. Assuming in a period T_s, (15) is written as a complex Fourier series:

$$s(t) = \sum_{k=0}^{\infty} X(k)e^{j2\pi kt/T_s} \tag{16}$$

To calculate the amplitude of the signal f_0, it requires

$$f_0 = m_0/T_s = m_0 f_s \tag{17}$$

where m_0 is an integer and f_s is the Fourier transform frequency, which means f_0 is the m_0th harmonic of the base frequency f_s .

The amplitude of the signal f_0 is

$$A_0 = X(m_0) = \frac{1}{T_s}\int_0^{T_s} s(t)e^{-j2\pi m_0 t/T_s}dt \tag{18}$$

To eliminate the influence of frequency f_{nom} , it should be

$$\int_0^{T_s}\cos(2\pi f_{nom}t+\varphi_1)e^{-j2\pi m_0 t/T_s}dt = 0 \tag{19}$$

It can be inferred that f_{nom} should comply with

$$f_{nom} = m_n/T_s = m_n f_s \quad (m_n \text{ is an integer}) \tag{20}$$

This conclusion means that the noise and signal frequencies are different harmonics of the base frequency f_s , which are orthogonal in the Fourier transform period. Such a communication principle is often used in the techniques such as Orthogonal Frequency-division Multiplexing (OFDM) and Minimum Shift Keying (MSK).

To minimize the frequency difference of the signal and noise, it is assumed that $m_n = m_0 \pm 1$, or

$$\triangle f = |f_{nom} - f_0| = \frac{1}{T_S} \tag{21}$$

If a three-carrier strategy is adopted, the frequency f_1 should be

$$\triangle f = |f_{nom} - f_1| = \frac{1}{T_S} \tag{22}$$

In this paper, the two-carrier strategy is employed because the switching frequency difference is smaller than that with the three-carrier strategy. To guarantee the data communication transparency, the traditional byte-based serial communication method is adopted, which adds a '0' and '1' at the beginning and end of the byte, respectively.

In the receiver, ripple signals pass through a low-pass filter to remove high-order harmonics before it connects to an ADC channel of a DSP. The cut-off frequency f_C of the low-pass filter and the sampling time f_{smp} should comply with the Nyquist theorem, or

$$f_{smp} > 2f_C \tag{23}$$

Assume N is the sample number in a Fourier transform period and is specified by

$$N = f_{smp}T_S \tag{24}$$

Fig.9 shows the relationship between sample frequency, noise frequency, and signal frequency.

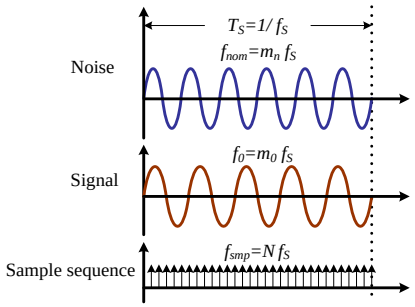


Fig.9 Waveforms of signal in a Fourier transform period.

The ripple signal sampled by the DSP is stored sequentially in memory, and then the DSP executes a discrete Fourier transformation (DFT) after each sample. The general DFT equation is

$$X(k) = \sum_{n=0}^{N-1} x(n)e^{-j\frac{2\pi}{N}nk} \quad (k = 0,1,...,N-1) \tag{25}$$

Letting $W = e^{-j\frac{2\pi}{N}K_0}$, the component of f_0 is

$$X_K = X(K_0) = \sum_{n=0}^{N-1} x(n)W^n \tag{26}$$

Assume that the current DFT value is based on the sequence $\{x(0), x(1),...x(N-1)\}$, and the next sequence is based on $\{x(1),$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2336628, IEEE Transactions on Industrial Electronics

$x(2),...x(N)\}$, an iterative method of sliding DFT can be employed [31], and the new DFT value after the next sample can be expressed as

$$X^*_K = \sum_{n=0}^{N-1} x(n+1)W^n = (\sum_{n=1}^{N} x(n)W^n)W^{-1} = [X_K - x(0) + x(N)]\ W^{-1} \quad (27)$$

Eqn.(27) decreases the DFT calculation time significantly, which makes it possible to execute the DSP DFT algorithm in every A/D sample period.

Assume that the effective signal received by each node is

$$x(t) = A_{nom}\cos(2\pi f_{nom}t + \theta_n)[1-c(t)] + A_0\cos(2\pi f_0 t + \theta_0)c(t) \quad (28)$$

where

$$c(t) = \begin{cases} 1 & \text{(if sending bit '0')} \\ 0 & \text{(no data or sending bit '1')} \end{cases}$$

The waveform shifts from f_{nom} to f_0 when $c(t)$ changes from '1' to '0' at t_0, and a window function $g(t)$ is defined as

$$g(t) = \begin{cases} 1 & (0 \le t \le T_s) \\ 0 & (t < 0 \ \text{ or } \ t > T_s) \end{cases} \quad (29)$$

Assume the period of a bit is more than T_s, the result of sliding sampling is $x(t,\tau)$

$$x(t,\tau) = \{A_{nom}\cos(2\pi f_{nom}t + \theta_n)[1-c(t)] + A_0\cos(2\pi f_0 t + \theta_0)c(t)\}g(t-\tau) \quad (30)$$

The f_0 component of $x(t,\tau)$ is

$$\begin{aligned} X_K(\tau) &= \int_{-\infty}^{\infty} x(t,\tau)e^{-j2\pi f_0 t}dt \\ &= \int_{\tau}^{\tau+T_s} \{A_{nom}\cos(2\pi f_{nom}t + \theta_n)][-c(t)] \\ &\quad + A_0\cos(2\pi f_0 t + \theta_0)c(t)\}e^{-j2\pi m_0 t/T_s}dt \end{aligned} \quad (31)$$

The amplitude of $X_k(\tau)$ can be inferred

$$\begin{aligned} |X_K(\tau)| &= \left|\int_{\tau}^{\tau+T_s} [-A_{nom}\cos(2\pi f_{nom}t + \theta_n) \right. \\ &\quad \left. + A_0\cos(2\pi f_0 t + \theta_0)]c(t)e^{-j2\pi m_0 t/T_s}\right| dt \\ &\begin{cases} = 0 & \text{if } c(\tau) = 0,\ (0 \le \tau \le T_s) \\ \le \frac{T_s}{2}(A_0\frac{\delta}{T_s} + \frac{A_0}{m_0} + \frac{2A_{nom}}{m_n}) & \text{if } \begin{pmatrix} c(\tau)=1 & (0 \le \tau \le \delta) \\ c(\tau)=0 & (\delta < \tau \le T_s) \end{pmatrix} \\ \le \frac{T_s}{2}[A_0(1-\frac{\delta}{T_s}) + \frac{A_0}{m_0} + \frac{2A_{nom}}{m_n}] & \text{if } \begin{pmatrix} c(\tau)=0 & (0 \le \tau \le \delta) \\ c(\tau)=1 & (\delta < \tau \le T_s) \end{pmatrix} \\ = A_0 T_s / 2 & \text{if } c(\tau) = 1,\ (0 \le \tau \le T_s) \end{cases} \end{aligned} \quad (32)$$

According to (27), the DFT result is refreshed every sampling period. When the sliding window function $g(t)$ coincides with the dedicated frequency f_0, the result reaches a maximum platform. Setting an appropriate threshold X_{th} or adopting more a complex judging algorithm, the data can be decoded. The process of demodulation is shown in Fig.10.

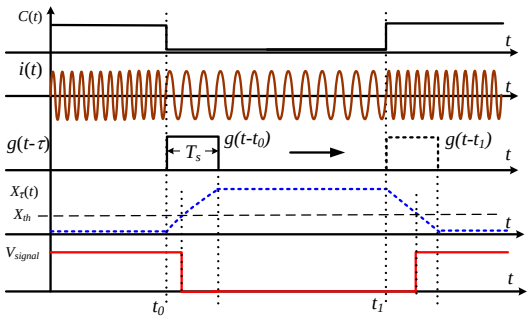


Fig.10 Schematic diagram of signal demodulation process.

V. Experiment Verification

A prototype system consisting five nodes is designed to verify the proposed method. The block diagram of the node is shown in Fig.11, which is based on conventional synchronic boost topology. The circuit is controlled by a DSP with related interface. The input current and output voltage are feedback for traditional close-loop control, and the ripple on the bus is filtered and amplified for signal decoding.

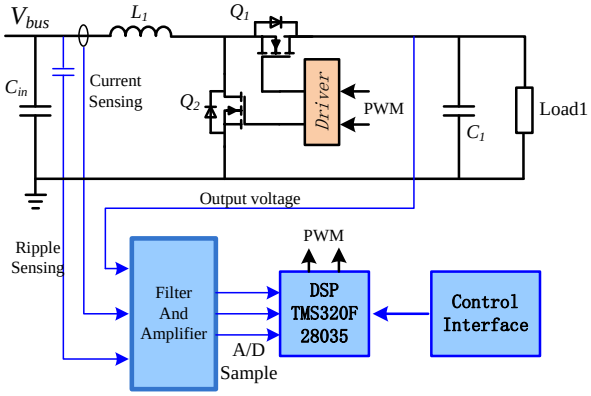


Fig.11 Block diagram of a node.

The prototype system structure is the same as shown in Fig.8 (a), where nodes are connected to the bus which is powered by a DC voltage source via an impedance stabilization network. All the nodes can communicate with each other.

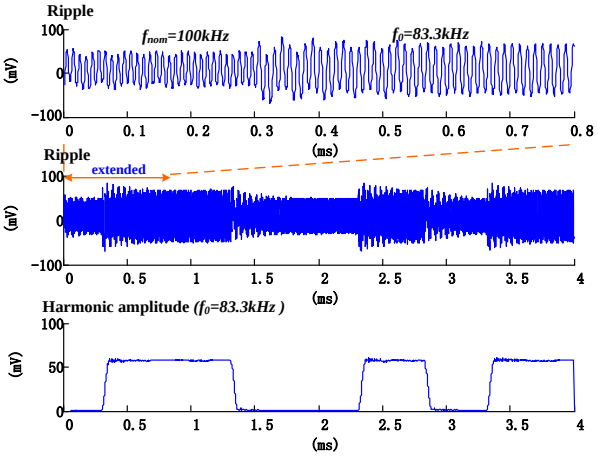
TABLE II.
SPECIFICATIONS OF PARAMETERS

Parameter of the Boost circuit	Value
V_{bus} (Input voltage)	10~15 V
V_{out} (Output voltage)	24 V
P_{out} (Maxim output power)	10W
L_1 (Boost inductor)	560 μH
C_{in} (Input capacitors)	2.2 μF
R_{s1} (ESR of C_{in})	30mΩ
f_{nom} (Switching frequency)	100kHz
f_0 (Switching frequency)	83.3kHz
T_{sample} (A/D sample period)	2μs
ADC resolution	12-bit
DFT period	60μs
Parameter of the Bus	**Value**
n (Number of Nodes)	5
Line length	2m
L_r (Impedance Matching Inductor)	10μH
C_r (Impedance Matching Capacitor)	2.2μF
R_r (ESR of Capacitor C_r)	30mΩ

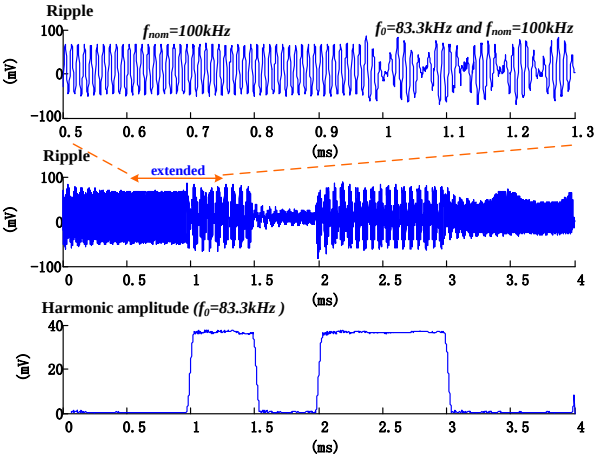
The system parameters are listed in Table. II, where the switching frequencies are selected as f_0=100kHz and

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2336628, IEEE Transactions on Industrial Electronics

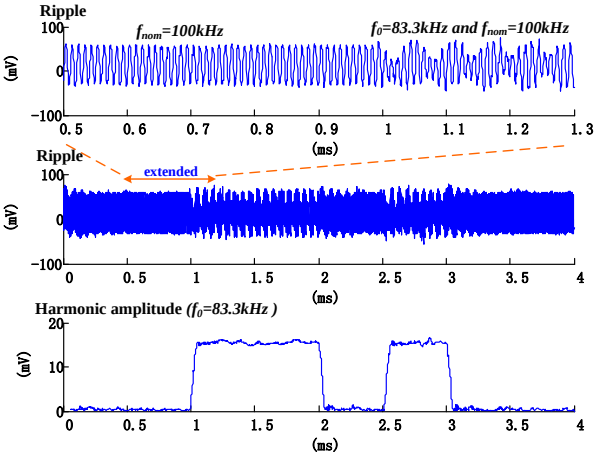
f_{nom}=83.3kHz, and the discrete Fourier transform period is 60μs during which f_0 and f_1 are orthogonal to one another. It can be calculated that m_0=6 and m_n=5. The DSP A/D sampling period T_{sample} is 2μs, so 30 words memory space is needed for DFT. The transmission rate is 2kbps, to realize reliable communications.



(a) One node installed on the bus.



(b)Two nodes installed on the bus.



(c) Five nodes installed on the bus.

Fig.12 Waveforms of ripple and the amplitude of the f_0 harmonic.

In the receiver, a band-pass Op amp filter is designed to amplify the data signal and decrease the high harmonic components, whose high-pass cut-off frequency is set about 150kHz. The output signal of the filter is about $1V_{p\text{-}p}$ and sampled by 12-bit ADC in the DSP TMS320F28035 every 2μs. According to (27), the f_0 (83.3kHz) component of the ripple is on-line calculated by the DSP. TMS320F28035 has a CLA (Control Law Accelerator) core with 32-bit float-point math accelerator by which DFT algorithm is implemented in assembly language, and the calculation time is less than 1μs.

The ripple waveform of one node installed on the bus is shown in Fig.12(a), The ripple frequency shifts between 100kHz and 83.3kHz. In most cases, the node employs 100kHz switching frequency except when sending bit '0'.

Fig.12(b) shows the ripple waveform and its DFT for two nodes operating on the bus, and Fig.12(c) shows the case for five nodes. If one node sends signal '0', the ripple on the bus is comprised of the components of f_0 and f_{nom}. The f_{nom} (100kHz) component on the bus is the synthesis of all nodes with different phases, so the amplitude is variable. However, the f_{nom} harmonic component will not affect the DFT result of f_0 frequency in the DFT conversion period.

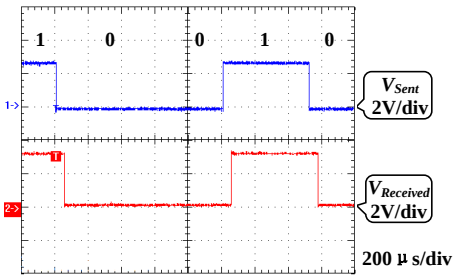


Fig.13 Waveforms of sent data and received data.

From Fig.12, as the number of nodes increases, the amplitude of the f_0 harmonic component reduces because the bus impedance decreases. If a constant threshold X_{Th} is set to distinguish valid communication signal from noise, the condition that n nodes can be supported by this system is

$$V_n > X_{Th} \tag{33}$$

where V_n is the DFT result of the f_0 component when n nodes operate on the bus. The value of X_{Th} is determined by the bus noise which is related to the design of signal processing circuits and power control loop.

Assume the capacitance of all the input capacitor C_k (k=1,2,…) in the nodes and the matching capacitor C_r are the same, it can be concluded that the maximum number of the system is

$$N_{\max} \le \frac{2V_1}{X_{Th}} - 1 \tag{34}$$

where V_1 is the DFT result of the f_0 component when one node operates on the bus.

Fig.13 shows the waveforms of the sent data of a node and the received data by another node. The bit width error between the sender and the receiver is no more than a DFT period (60μs), so it is reliable for a serial communication rate of 2kbps. To implement a bus communication system with multiple nodes, it is necessary to exploit a Multiple Access Control (MAC) protocol for application, which is beyond the scope of this paper.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2336628, IEEE Transactions on Industrial Electronics

VI. CONCLUSIONS

This paper presents a method of power/signal dual modulation (PSDM) to integrate data transmission with power conversion. In the proposed PSDM system, the information is embedded into the ripple of the converter. By analyzing the waveform of the ripple, communication between nodes can be realized.

Two basic methods for PSDM are proposed, namely PWM/FSK and PWM/PSK. The modulation and demodulation process of PWM/FSK are discussed in detail and a prototype system is used to verify the technique. Two principles are concluded: firstly, topology and carrier may be constraints on the PSDM system. The boost converter circuit is suitable for PSE while the buck circuit is suitable for PD. A triangle wave is better carrier option since a sawtooth carrier introduces an additional interference problem. Secondly, the carrier frequencies should be orthogonal within a calculation period, and the difference of the shifting frequency is related to the communication rate. The closer the shifting frequencies, the slower communication rate.

This method proposes a way of designing an 'intelligent power supply' which can send messages from the control core. The technique can be applied in distributed power systems or some special powering arrangements. However, some problems should be considered before use. First, the ripple utilized to communication should comply with EMI standards which restrict the amplitude of the harmonic frequencies; second, this method is not suitable for critical situations such as communication-based control systems; third, the effect of cross-interference between power control and signal transmission was not analyzed, and may cause communication data error, but this problem can be overcome by adding an Automatic Repeat Request (ARQ) mechanism into the communication protocol.

REFERENCES

[1] A. Iera, C. Floerkemeier, J. Mitsugi, and G. Morabito, "The Internet of things [Guest Editorial]," *IEEE Wirel. Commun.*, vol.17, no.6, pp.8–9, Dec. 2010.

[2] E. I. Gaura, J. Brusey, M. Allen, R. Wilkins, D. Goldsmith, and R. Rednic, "Edge mining the Internet of things," *IEEE Sens. J.*, vol.13, no.10, pp.3816–3825, Oct.2013.

[3] D. Guinard, V. Trifa, S. Karnouskos, P. Spiess, and D. Savio, " Interacting with the SOA-based Internet of things: discovery, query, selection, and on-demand provisioning of web services," *IEEE Trans. Services Comput.*, vol.3, no.3, pp.223–235, Jul.-Sept. 2010.

[4] Q. Wang, S. Gopalakrishnan, "Adapting a main-stream Internet switch architecture for multihop real-time industrial networks," *IEEE Trans. Ind. Inf.*, vol.6, no.3, pp.393–404, Aug.2010.

[5] A.C.Weaver, M.W. Condry, "Distributing Internet services to the network's edge," *IEEE Trans. Ind. Electron.*, vol.50, no.3, pp.404–411, June 2003.

[6] C. W. Thompson, "Smart devices and soft controllers," *IEEE Internet Computing*, vol.9, no.1, pp.82–85, Jan.-Feb.2005.

[7] J. M. Guerrero, Lijun Hang, and J. Uceda, "Control of distributed uninterruptible power supply systems," *IEEE Trans. Ind. Electron.*,vol.55, no.8, pp.2845–2859, Aug.2008.

[8] V. C. Gungor, D. Sahin, T. Kocak, S. Ergut,C. Buccella, C. Cecati, and G. P. Hancke, "A survey on smart grid potential applications and communication requirements," *IEEE Trans. Ind. Inf.*, vol.9, no.1,pp.28–42, Feb.2013.

[9] S. K. Mazumder, M. Tahir, and K. Acharya, "Master–slave current-sharing control of a parallel DC–DC converter system over an RF communication interface," *IEEE Trans. Ind. Electron.*, vol.55, no.1, pp.59–66, Jan. 2008.

[10] E. J. Bueno, A. Hernández, F. J. Rodríguez, C. Girón, R. Mateos, and S. Cóbreces, "A DSP and FPGA-based industrial control with high-speed communication interfaces for grid converters applied to distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol.56, no.3, pp.654–669, Mar.2009.

[11] T. Sauter, "The three generation of field-level networks-evolution and compatibility issues," *IEEE Trans. Ind. Electron.*, vol.57, no.11, pp.3585–3595, Nov. 2010.

[12] B. Groza, and S. Murvay, "Efficient protocols for secure broadcast in controller area networks," *IEEE Trans. Ind. Inf.*, vol.9, no.4, pp.2034–2042, Nov. 2013.

[13] A. Flammini, D. Marioli, E. Sisinni and A. Taroni, "Design and implementation of wireless fieldbus for plastic machineries," *IEEE Trans. Ind. Electron.*, vol.56, no.3, pp.747–755, Mar.2009.

[14] M., Sechilariu, B. Wang, F. Locment, "Building integrated photovoltaic system with energy storage and smart grid communication," *IEEE Trans. Ind. Electron.*,vol. 60, no. 4,pp. 1607–1618, Apr. 2013

[15] Y. Ishii, "Exploiting backbone routing redundancy in industrial wireless system," *IEEE Trans. Ind. Electron.*, vol.56, no.10,pp.4288–4295, Oct.2009.

[16] E. M. Shakshuki, N. Kang, and T. R. Sheltami, "EAACK-A secure instruction-detection system for MANETs," *IEEE Trans. Ind. Electron.*,vol.60, no.3,pp.1089–1098, Mar.2013.

[17] C. Alcaraz and J. Lopez, "A security analysis for wireless sensor mesh network in highly critical system," *IEEE Trans. Syst., Man, Cybern.C: Appl. Rev.*,,vol.40, no.3,pp.419–428, Jul.2010.

[18] J.J. Fahie, "Edward Davy," *The Electrician*, pp. 181–227, July, 1883.

[19] T. A. Papadopoulos, C. G. Kaloudas, A. I. Chrysochos, and G. K. Papagiannis, "Application of narrowband power-line communication in medium-voltage smart distribution grids," *IEEE Trans. Power. Del.*,vol.28, no.2,pp.981–988, Apr.2013.

[20] H. Meng, S. Chen, Y. L. Guan, C. L. Law,P. L. So, E. Gunawan, and T. T. Lie, "A transmission line model for high-frequency power line communication channel," in *Proc. 5th Int. Conf. Power Syst. Technol.*, Kunming, China, Oct. 2002, vol. 2, pp. 1290–1295.

[21] M. A. Mannah, N. Ginot, and C. Batard, "Effect of the power cable on data transmission over a pulsewidth-modulated network," *IEEE Trans. Ind. Electron.*,vol.61, no.8,pp.4238–4245, Aug, 2014.

[22] N. Pavlidou, A. J. Han Vinck,J. Yazdani, and B. Honary, "Power line communications: state of the art and future trends," *IEEE Commun. Mag.*, vol.41, no.4, pp34–40, Apr. 2003.

[23] V., K. Kilani, L. Konéé, M. Liénard, and P. Degauque, "Feasibility of a high-bit-rate power-line communication between an inverter and a motor," *IEEE Trans. Ind. Electron.*,vol.61, no.9, pp4816–4823, Sep., 2014.

[24] T. Sauter and M. Lobashov, "End-to-End Communication Architecture for Smart Grids," *IEEE Trans. Ind. Electron.*,vol.58, no.4, pp1218–1228, Apr. 2011.

[25] J. Liu, B. Zhao, J. Wang,Y. Zhu, and J. Hu, "Application of power line communication in smart power Consumption," in *Proc. IEEE ISPLC*, Mar. 2010, pp.303–307.

[26] H. Kubota, K. Suzuki, I. Kawakami,M. Sakugawa, and H. Kondo, "High frequency band dispersed-tone power line communication modem for networked appliances," *IEEE Trans. Consum. Electron.*, vol.52, no.1, pp. 44–50, Feb. 2006.

[27] C. Lin, H. Chu, S. Yeh,M. Lu, J. Yao, and H. Chen, "Robust video streaming over power lines," in *Proc. Int. Symp. Power Line Commun. Appl.*, Orlando, FL, 2006, pp196–201.

[28] W. Stefanutti, P. Mattavelli, S. Saggini, andL. Panseri, "Communication on power lines using frequency and duty-cycle modulation in digitally controlled DC-DC converters," in *Proc. IEEE IECON*, Paris, France, 2006, pp.2144–2149.

[29] W. Stefanutti, S. Saggini, P. Mattavelli and M. Ghioni, "Power line communication in digitally controlled DC-DC converters using switching frequency modulation," *IEEE Trans. Ind. Electron.*, vol.55, no.4, pp.1509–1518, Apr. 2008.

[30] C.D.Xu andK.W.E.Cheng, "A survey of distributed power system - AC versus DC distributed power system," in *Proc. Conf. Power Electron. Syst Appl.*,Hong Kong, 2011,pp.1–12.

[31] E. Jacobsen and R. Lyons, "The sliding DFT," *IEEE Signal Process. Mag.*, vol.20, no.2, pp.74–80, Mar. 2003.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TIE.2014.2336628, IEEE Transactions on Industrial Electronics

Jiande Wu (M'11) was born in Zhejiang, China, in 1973. He received the B.Sc., M.SC and Ph.D. degree from the College of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1994, 1997 and 2012, respectively. Since 1997, he has been a faculty member at Zhejiang University, where he is currently an associate professor. From 2013 to 2014, he was an academic visitor at the University of Strathclyde, Glasgow, U.K. His research interests include power electronics control, distributed power electronics system and fieldbus communication.

Jin Du (S'11) received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2011. Currently, he is working toward the Ph.D. degree in the College of Electrical Engineering, Zhejiang University, China. His current research interests include power optimization of renewable generation and communication technique applied in power electronics.

Zhengyu Lin (S'03–M'05–SM'10) received the B.Sc.and M.Sc. degrees from the College of Electrical Engineering, Zhejiang University, Hangzhou, China, in 1998 and 2001, respectively, and the Ph.D. degree from Heriot-Watt University, Edinburgh, U.K.,in 2005. He is currently a Lecturer in Electrical, Electronic and Power Engineering with Aston University, Birmingham, U.K. He was a Research Associate with the University of Sheffield from 2004 to 2006, an R&D Engineer with Emerson Industrial Automation, Control Techniques PLC from 2006 to 2011, a Senior Research Scientist with Sharp Laboratories of Europe Ltd. from 2011 to 2012, and a Lecturer with Coventry University from 2013 to 2014. His research interests include power electronics and its applications in renewable energy, energy storage, motor drives and power systems.

Yihua Hu (M'13) received the B.S. degree in electrical motor drives in 2003, and the Ph.D. degree in power electronics and drives in 2011, both from China University of Mining and Technology, Jiangsu, China. Between 2011 and 2013, he was with the College of Electrical Engineering, Zhejiang University as a Postdoctoral Fellow. Between November 2012 and February 2013, he was an academic visiting scholar with the School of Electrical and Electronic Engineering, Newcastle University, Newcastle upon Tyne, UK. He is currently a research associate with the Department of Electronic & Electrical Engineering, University of Strathclyde, Glasgow, UK. He has published more than 20 technical papers in leading journals and conference proceedings. His research interests include PV generation system, DC-DC/DC-AC converters, and electrical motor drives.

Chongwen Zhao (S'13) received the B.Sc. degree from the School of Electronic Engineering, Xidian University, Xi'an, China, in 2011, and received the M.Sc. degree from the College of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2014. Currently, he is working toward the Ph.D. degree in electrical engineering at the University of Tennessee, Knoxville, TN, USA. His research interests include wireless power and communication applications, DC-DC power conversions.

Xiangning He (M'95–SM'96–F'10) received the B.Sc. and M.Sc. degrees from the Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 1982 and 1985, respectively, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 1989. From 1985 to 1986, he was an Assistant Engineer with the 608 Institute of Aeronautical Industrial General Company, Zhuzhou, China. From 1989 to 1991, he was a Lecturer with Zhejiang University. In 1991, he received a Fellowship from the Royal Society of U.K. and conducted research in the Department of Computing and Electrical Engineering, Heriot-Watt University, Edinburgh, U.K., as a Postdoctoral Research Fellow for two years. In 1994, he joined Zhejiang University as an Associate Professor, where he has been a Full Professor since 1996. He is currently the Vice Dean of the College of Electrical Engineering, Zhejiang University. His research interests include power electronics and their industrial applications.