

# NEW BACK-TO-BACK CURRENT SOURCE CONVERTER WITH SOFT START-UP AND SHUTDOWN CAPABILITIES

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## Abstract

Back-to-back voltage source and current source converters are key components of many power conversion systems. Various topologies have evolved around these conventional voltage and current source converters in an attempt to meet different design and reliability constraints. This paper proposes a new back-to-back current source converter that avoids the problem of excessive voltage stresses on the switching devices associated with the traditional current source converter. Its main features are reduced power circuit and control complexity, and sinusoidal ac currents with high power factor achieved at both ac sides at reduced switching frequency. Basic relationships that govern steady-state converter operation are established, and filter design is included. PSCAD/EMTDC simulations and experimentation are used to demonstrate the practicality of the proposed power conversion system, and results show that the converter has good dynamic performance, with near unity input power factor over an extended operating range.

## 1 Introduction

Back-to-back (BTB) converters are used in many power conversion applications, such as machine drives, wind energy systems, uninterruptible power supplies and HVDC transmission systems. Various topologies have evolved around voltage source converters (VSC) and current source converters (CSC) in an attempt to meet various design and reliability constraints [1]. The conventional BTB converter consists of a rectifier and an inverter connected via an energy storage element such as a capacitor for a VSC or an inductor for a CSC [2].

The VSC based BTB has a faster dynamic response and higher efficiency than the BTB CSC [3, 4], whilst the CSC in a BTB arrangement has higher reliability and inherent current limiting capability during dc faults [5-7].

A new CSC based BTB power conversion system that is suitable for a wide range of medium-voltage applications is presented. It addresses the main limitations of conventional CSC based power converters, such as the over-voltage frequently experienced by switches during commutation. Additionally, it offers improved ac side waveforms, reduced

semiconductor power loss, and soft start-up and shutdown by exploiting its buck and boost capability.

## 2 Proposed back-to-back converter

### 2.1 Operating principle

Figure 1 shows the proposed BTB converter. It consists of a three-phase bridge rectifier and associated ac filters ( $L_s$  and  $C_s$ ) at the source side, and a three-phase current source inverter (CSI) with its ac filter capacitor  $C_i$  at the load side. Series switch  $S_r$  is placed between the rectifier bridge and the dc-link inductor  $L_{dc}$  to adjust the output current by controlling the average current flow in the link inductor and, hence, the power flow between the source and three-phase load.

The switching period,  $T=t_1+t_2$ , of switch  $S_r$  is divided into two operating modes. The first mode is the dc-link inductor ( $L_{dc}$ ) charging mode where switch  $S_r$  is turned on during the interval  $0 \leq t \leq t_1$ . In this mode, dc-link inductor current  $I_L$  rises to equal switch current  $I_s$ , whilst the input current,  $I_i$ , to the CSI is equal to zero. The second mode is where switch  $S_r$  is turned off during the period  $t_1 \leq t \leq t_2$ . In this mode, the dc-link inductor current  $I_L$  gradually decreases as the energy stored in  $L_{dc}$  during the first mode is transferred to the load, so that  $I_L=I_i$  and  $I_s=0$ . The relationships between the average dc-link inductor current  $\bar{I}_L$ , average switch current  $\bar{I}_s$  and average CSI input current  $\bar{I}_i$  can be summarised as shown in Equations (1) and (2):

$$\bar{I}_i = (1 - \delta)\bar{I}_L \quad (1)$$

$$\bar{I}_s = \delta\bar{I}_L \quad (2)$$

where  $\delta=t_1/T$  is the switch on-state duty cycle such that  $0 \leq \delta \leq 1$ .

The proposed BTB converter is operated such that it controls the load power by modulating average input dc-link current  $\bar{I}_i$ . Although  $I_i$  is discontinuous, its average value over the fundamental period is constant. For minimum switching losses, the CSI is controlled using selective harmonic elimination (SHE) PWM, with three notches per quarter cycle to adjust fundamental current and eliminate the 5<sup>th</sup> harmonic current. The switching frequency  $f_{sr}$  of switch  $S_r$  is 2.4kHz and the required output frequency  $f_{op}$  is 50Hz. To ensure zero switching losses in the CSI, the switching instants of the CSI devices must coincide with zero input dc link current  $I_i$ , which is determined by the modulation of switch  $S_r$ .

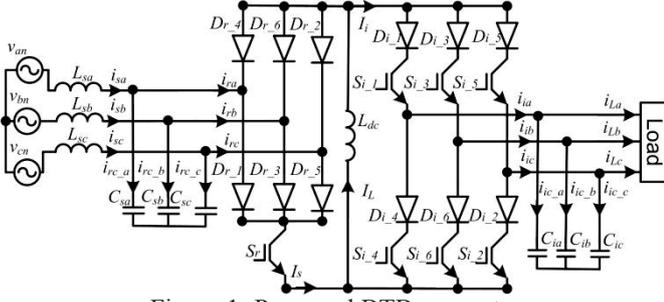


Figure 1: Proposed BTB converter

## 2.2 Circuit analysis

Figure 2 shows a simplified representation of the proposed BTB converter. By applying the current divider method to the load side, the relationship between fundamental per-phase rms CSI output current  $|i_i|$  and fundamental per-phase rms load current  $|i_L|$  is:

$$|i_L| = \frac{1}{|1 + j\omega_{op} C_i Z_L|} |i_i| \quad (3)$$

where  $\omega_{op}$  is the output frequency in rad/s and  $Z_L$  is load impedance.

SHE PWM is used to eliminate the 5<sup>th</sup> harmonic from the CSI output current. At modulation index equal to 1, the peak fundamental CSI output current equals the average CSI input current, i.e.  $\bar{I}_i = \sqrt{2}|i_i|$ . From Equation (1), Equation (3) can be rewritten in terms of the dc-link inductor current as:

$$|i_L| = \frac{(1-\delta)\bar{I}_L}{\sqrt{2}|1 + j\omega_{op} C_i Z_L|} \quad (4)$$

To facilitate analysis of the rectifier input current, the dc side inductance  $L_{dc}$  is assumed sufficiently large so that the dc side inductor current is constant (ripple free) and equals  $\bar{I}_L$ . Figure 3 shows rectifier input current during one fundamental cycle. The spectrum of the rectifier input current  $i_r$  can be obtained using the double Fourier series in complex form [8]:

$$i_{r-mn} = \frac{1}{2\pi^2} \left[ \int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} \int_{-\delta\pi}^{\delta\pi} \bar{I}_L e^{j(mx+ny)} dx dy + \int_{\frac{5\pi}{6}}^{\frac{11\pi}{6}} \int_{-\delta\pi}^{\delta\pi} \bar{I}_L e^{j(mx+ny)} dx dy \right] \quad (5)$$

where  $y = \omega_0 t$  and  $x = \omega_c t$ ,  $\omega_0$  and  $\omega_c$  respectively represent the fundamental and carrier frequencies in rad/s, and where  $m$  and  $n$  respectively are the orders of the carrier and baseband component harmonics.

The baseband harmonics of the rectifier input current  $i_r$  are computed by setting  $m=0$  in Equation (5), yielding:

$$i_{r-0n} = A_{0n} + jB_{0n} = \frac{j2\sqrt{3}\delta\bar{I}_L}{n\pi} \quad (6)$$

Equation (6) is valid for all  $n$  that represent odd and non-triplen harmonics, otherwise  $i_{r,0n} = 0$  so that  $A_{0n} = 0$  and  $B_{0n} = \frac{2\sqrt{3}\delta\bar{I}_L}{n\pi}$ . The peak value of the rectifier input fundamental component  $i_{r-p}$  is obtained with  $n=1$ , so that:

$$i_{r-p} = \frac{2\sqrt{3}\delta\bar{I}_L}{\pi} \quad (7)$$

The rms value of the rectifier input fundamental current component  $|i_r|$  is:

$$|i_r| = \sqrt{6} \frac{\delta\bar{I}_L}{\pi} \quad (8)$$

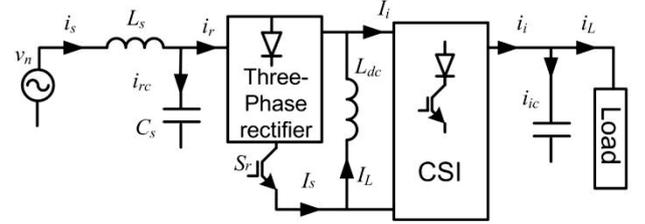


Figure 2: Simplified representation of the proposed converter

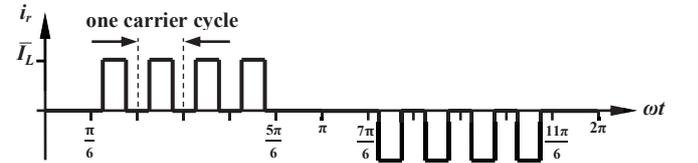


Figure 3: Rectifier input current during one carrier cycle

Assuming lossless conversion, power balance dictates that input power to the converter equals the output power:

$$3|i_r||v_{cs}| = 3|i_L|^2 R_L \quad (9)$$

where  $|v_{cs}|$  is the rms fundamental phase voltage across the rectifier side capacitors, and  $R_L$  is the per-phase load resistance. By substituting Equation (8) into Equation (9):

$$|v_{cs}| = \frac{\pi}{\sqrt{6}\delta\bar{I}_L} |i_L|^2 R_L \quad (10)$$

The corresponding rms fundamental supply current  $|i_s|$  can be expressed as:

$$|i_s| = \frac{|v_{cs} - v_n|}{2\pi f_s L_s} \quad (11)$$

where  $f_s$  is the supply frequency.

## 2.3 Supply side filter design

The phase current conduction period of the source side converter is  $\frac{2}{3}\pi$  radians per half-cycle, making its filter design more challenging. Equation (6) has shown that the converter input current  $i_r$  contains all odd and non-triplen harmonics: dominantly the 5<sup>th</sup> and the 7<sup>th</sup>. To attenuate these dominant harmonics, the ac side filter cut-off frequency is initially selected to be 2.5 times the supply frequency  $f_s$ . Input filter capacitance  $C_s = 0.33\mu$  is adopted, which is within the normal range for a high-power, low switching frequency PWM CSC [9]. Simulation results for different operating conditions show, however, that for acceptable supply current THD, the ac filter cut-off frequency must be  $2.4f_s$ . The ac side filter inductor  $L_s$  is therefore designed using Equations (12) and (13):

$$2.4\omega_B = \frac{1}{\sqrt{L_s C_s}} \quad (12)$$

$$L_s = \frac{1}{5.76\omega_B^2 C_s} \quad (13)$$

where  $\omega_B$  is the base frequency in rad/s, base capacitance  $C_B = \frac{1}{\omega_B Z_B}$ , base inductance  $L_B = \frac{Z_B}{\omega_B}$  and  $Z_B$  is the base impedance [10]. Therefore:

$$L_s = \frac{1}{5.76\omega_B^2 \left(\frac{0.33}{\omega_B Z_B}\right)} = \frac{Z_B}{1.9\omega_B} = 0.53L_B \quad (14)$$

Equations (15) and (16) express the ac side filter parameters in terms of the rated line-to-line voltage  $V_{LL}$  and rated input power  $P$  for star configuration, while Equation (17) specifies the filter capacitance  $C_s$  for the delta configuration.

$$L_s = 0.53 \frac{V_{LL}^2}{2\pi f P} \quad (15)$$

$$C_s = 0.33 \frac{P}{2\pi f V_{LL}^2} \quad (16)$$

$$C_s = 0.11 \frac{P}{2\pi f V_{LL}^2} \quad (17)$$

Based on simulations and experimentation, it has been shown that with the filter values calculated based on Equations (15) and (16), the input power factor profile of the proposed BTB converter varies with the input power as shown in Figure 4. The figure shows that the input power factor exceeds 0.8 between 0.4pu and 1pu rated load.

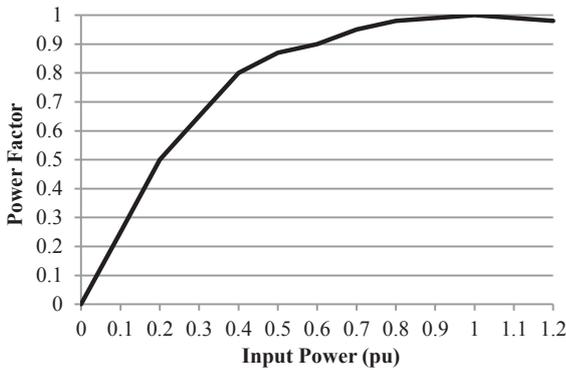


Figure 4: Supply current power factor profile

## 2.5 Controller design

Since the proposed BTB power conversion system supplies an isolated three-phase load, the strategy shown in Figure 5 is adopted for switch control. The outer loop regulates the voltage magnitude across the load and sets the reference average dc link inductor current  $\bar{I}_{L\_ref}$ . A current limiter stage is used to protect the power electronic components from over-current. The inner current control loop regulates  $\bar{I}_L$  and estimates modulation index  $\delta$  for the active switch  $S_r$ .

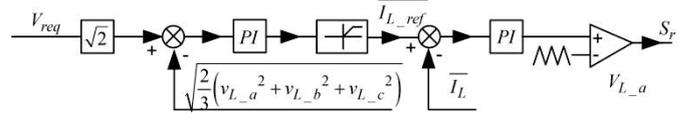


Figure 5: Control loop

## 3 Simulations

The proposed BTB converter having the parameters listed in Table 1 is simulated. To demonstrate system soft start-up, the reference voltage at the load terminals is increased gradually from zero to rated voltage. To test the dynamic performance of the proposed BTB system, a load step change is applied at time  $t=1s$  by connecting an additional parallel resistive load of  $18\Omega$ . The results of these tests are shown in Figure 6 to Figure 10. Figure 6 shows that the voltage across the load is maintained constant at  $311V_{pk}$  ( $220V_{rms}$ ) as the load is varied. Figure 7 shows that as the load increases the average dc-link current and its reference ( $\bar{I}_{L\_ref}$ ) increase to maintain power balance between the ac and dc sides. Figure 8 shows that the step change in load causes the converter input power to increase from 15kW (0.75pu) to 23kW (1.15pu). Figure 9 shows supply currents and phase 'a' voltage as load varies, and highlights that the input power factor is in agreement with the theoretical values shown in Figure 4. Figure 10 shows the load current during the step change in load and highlights the proposed BTB converter's ability to continue supply of sinusoidal current to the load.

Rated input power	20kW
Supply voltage	$208V_{LL}$
Supply frequency	60Hz
Rectifier side filter inductance	3mH
Rectifier side filter capacitance	$130\mu F$ ( $\Delta$ connection)
DC link inductance	5mH
Output frequency	50Hz
Inverter side filter capacitance	$130\mu F$ ( $\Delta$ connection)
Load resistance	$10\Omega$
Load inductance	4mH

Table 1: Simulation parameters

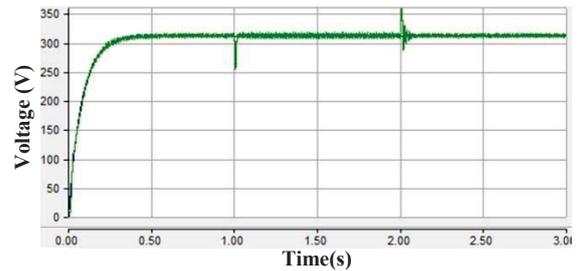


Figure 6: Peak output load voltage

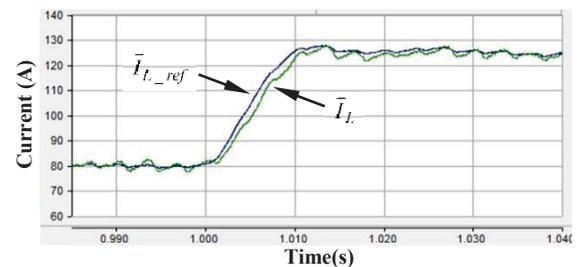


Figure 7: Average dc-link inductor current during load step

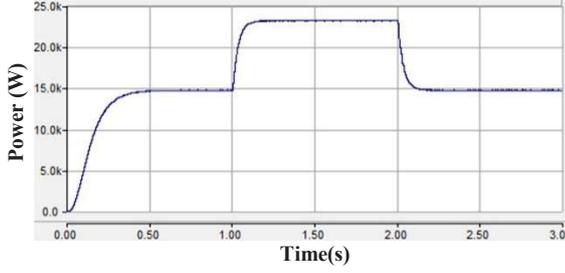


Figure 8: Converter input power

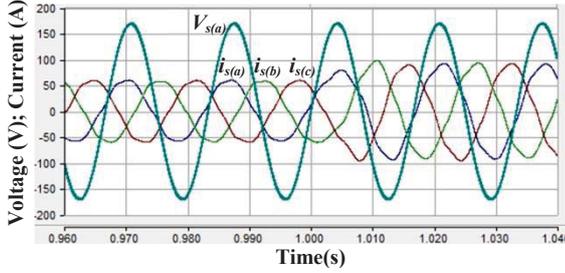


Figure 9: Supply current during step load increase

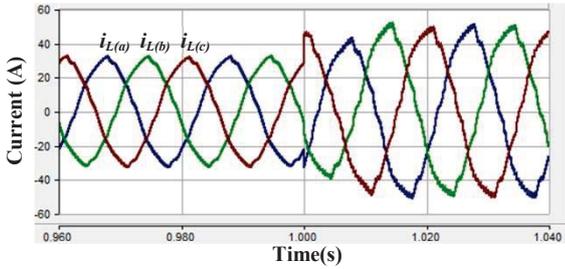


Figure 10: Load current during step load increase

## 4 Experimental validation

Results obtained from a scaled-down experimental test rig of the proposed BTB, with parameters listed in Table 2, are presented. Unlike with the simulation described in Section 3, the output voltage reference is changed to initiate a step change in the load. To enable soft start-up and soft change, the reference voltage is passed through a low-pass filter with cut-off frequency of 2Hz. Initially the output voltage reference is set to  $75V_{pk}$  and then increased to  $90V_{pk}$ , corresponding to measured input powers of 380W and 840W respectively. Figure 11 and Figure 12 show the three-phase supply currents and phase 'a' voltage with output voltage references of  $75V_{pk}$  and  $90V_{pk}$  respectively. These figures show that the supply currents are sinusoidal and that power factor changes from 0.8 leading to unity as the reference is increased. Figure 13 and Figure 14 show load voltage build-up during black-start and during a change in load voltage reference, demonstrating the ability of the proposed BTB power conversion system to operate in islanding mode. Figure 15 shows that the current source converter presents sinusoidal output voltages to the load.

## 5 Conclusions

A new current source based back-to-back power conversion topology for medium voltage applications is presented.

Theoretical analysis, simulations, and experimental results have shown that the proposed power conversion system offers several advantages such as soft start-up and shutdown, high efficiency, and fast dynamic performance. The presented ac side filter design ensures high power factor at rated power, and low input current THD at the rectifier side.

Rated input power	840W
Supply voltage	$50V_{L-L}$
Supply frequency	50Hz
Rectifier side filter inductance	5mH
Rectifier side filter capacitance	$120\mu F$ ( $\Delta$ connection)
DC-link inductance	5mH
Output frequency	50Hz
Inverter side filter capacitance	$90\mu F$ ( $\Delta$ connection)
Load resistance	$25\Omega$
Load inductance	3.3mH

Table 2: Experimental parameters

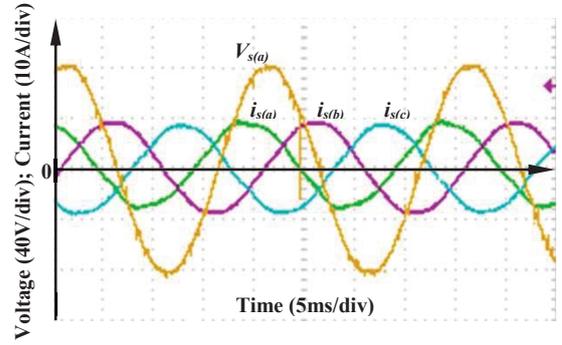


Figure 11: Detailed view of three-phase supply currents and phase 'a' voltage when output voltage reference is  $75V_{pk}$

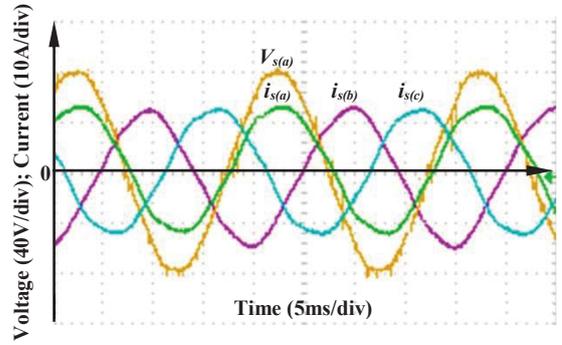


Figure 12: Detailed view of three-phase supply currents and phase 'a' voltage when output voltage reference is  $90V_{pk}$

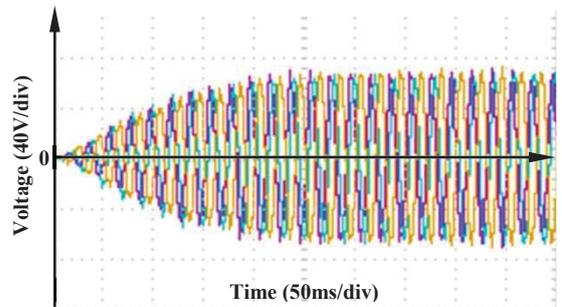


Figure 13: Output voltage during start up

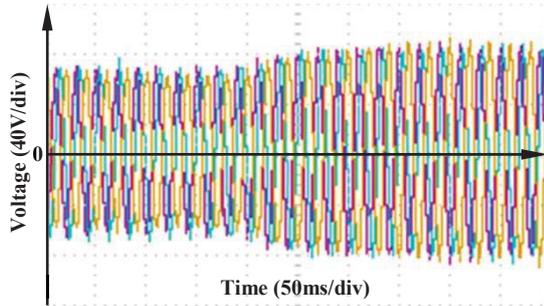


Figure 14: Output voltage during an increase in reference

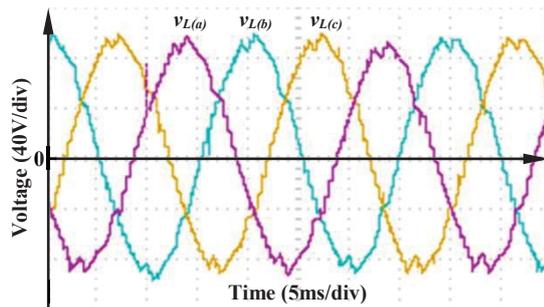


Figure 15: Detailed view of three-phase output voltage following an increase in reference

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