Modular input-parallel-output-series DC/DC converter control with fault detection and redundancy

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Abstract

Large offshore wind farms will require an extensive sub-sea power network to provide internal interconnection. Present solutions are based around conventional medium-voltage AC architectures. This paper proposes an alternative DC collection network based around modular DC/DC converters with input-parallel-output-series (IPOS) connection. Small-signal analysis of the converter is presented, to assist in control scheme development for the converter input and output stages. A Lyapunov controller is embedded within the conventional output voltage sharing control loop. A master-slave control scheme is proposed to ensure power sharing under a range of operating conditions, and provides fault-tolerant operation since the status of 'master' can be reallocated in the event that the present 'master' module fails.

1 Introduction

In comparison with an AC network, a DC collection grid offers a number of potential benefits. The use of DC can better utilise the cable voltage rating and eliminates the charging current associated with long AC cables. These issues may become of increasing importance as the capacity and area of offshore wind farms increase. A medium-voltage DC collection grid also has the potential to reduce losses through the use of medium-voltage converters and better optimisation of conversion stages [1]. Additionally, a DC collection grid may reduce the size and weight of the required plant and power units [1]. Present offshore farms connect to conventional 50 or 60Hz AC systems by employing mains-frequency transformers to step up the generator output voltage to collection network voltage levels. Advances in DC/DC converters, particularly High-Frequency (HF) technologies [2, 3], allow the heavy line-frequency transformer in an AC grid to be replaced by a high- or medium-frequency transformer, leading to significant weight and size savings.

Fig.1 illustrates AC and DC options for the collection grid. In a DC collection grid, each individual wind turbine outputs DC from a fully rated DC/DC converter that replaces the conventional DC/AC stage of the back-to-back converter. Currently, there is uncertainty regarding the architectures and control approaches that enable this high-capacity DC/DC power conversion. One possible solution is to use modular multilevel DC/DC converter (MMC) technology which has been widely studied for HVDC and MVDC [4, 5]. Modular multilevel approaches to high-voltage conversion have achieved significant gains in HVDC applications. The effectiveness of such techniques is, however, limited in DC/DC applications [4, 5]. Instead, a more compact and lighter design that uses a few modules arranged in a parallel-series topology could provide a replacement for a conventional single converter that uses high-voltage valves comprising several series-connected switching devices to enable operation at medium-voltage. In contrast to the topology where a single converter is managing all the power, in IPOS connected-converter the power is equally shared by all the modules.

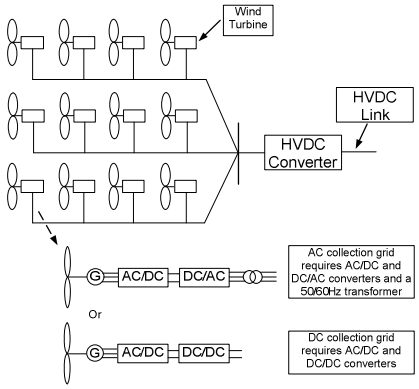


Fig.1 Offshore wind farm AC and DC collection grids

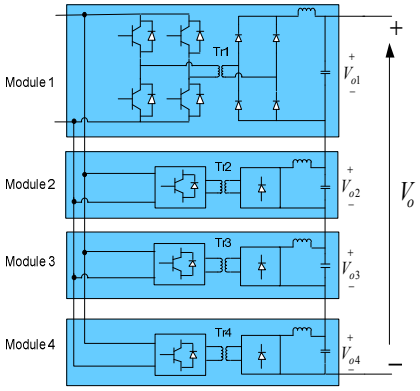


Fig.2 IPOS converter system topology

Fig.2 shows the layout of the proposed input parallel output series compact modular DC/DC converter topology with a 4-

module example. The proposed converter has an input parallel connection to provide current sharing, with each module being subjected to reduced current stress. This, in turn, simplifies converter design and manufacture. The series connection of the high-voltage side supports the collection network voltage. The modularity feature allows distribution of power management requirement among multiple modules. The modular architecture offers other advantages such as internal fault tolerance, as a result of (n+k) designed redundancy, and reduced filter size resulting from interleaved control [13-16].

Currently, the open literature contains few publications in the field of the IPOS converter and its control strategy. Normally, the average active sharing method or the master-slave active sharing method is chosen to solve the power sharing issue under any steady-state condition with mismatched components among the modules, and other challenging conditions such as inconformity of the transfer function, switching delay and discontinuity caused by the switching time delay, and input voltage disturbance [6]. In the master-slave control method, the master module is responsible for load regulation whilst the slaves ensure equal current and voltage sharing among the modules. Compared to the average active sharing method, fault-ride-through under module failure may be achieved more simply using master-slave control, with input current and output voltage being evenly shared among the remaining healthy modules. For existing control schemes, fault detection and protection methods for input-parallel-output-series connected DC/DC converters are not reported in the literature.

This study presents a control strategy based on a 'master-slave' scheme that enables power sharing between modules in an IPOS DC/DC converter under any steady-state condition where there is mismatch between module components, and which achieves ride-through of internal faults such as module failure. The proposed control scheme avoids the problems associated with ensuring (n+1) redundancy in the event of a fault in the master module that are characteristic of fixed 'master-slave' control schemes.

The paper is organised as follows: Controller design for an IPOS connected system with a full-bridge (FB) DC/DC converter is presented in Section 2. The response of the control system to abnormal fault conditions is also analysed, and a fault detection and protection scheme is proposed and presented. Section 3 presents the simulation results and the conclusions are presented in Section 4.

2 Control Theory

2.1 Small-Signal Modelling of an IPOS-Connected DC/DC Converter

The efficiency of each module is assumed to be 100% and there are n modules in total. The relationship between input and output power can be obtained for each module:

$$\begin{cases} V_{in}I_{in1} = V_{o1}I_o \\ V_{in}I_{in2} = V_{o2}I_o \\ \quad\bullet \\ \quad\bullet \\ \quad\bullet \\ V_{in}I_{inn} = V_{on}I_o \end{cases} \tag{1}$$

where V_{in} is the DC input voltage, I_{in1}, I_{in2},…, I_{inn} are the module input currents, V_{o1}, V_{o2},…, V_{on} are the module output voltages, and I_o is the load current. In the steady-state condition, the average filter capacitor current is zero. The filter inductor current ripple is therefore very small. If output voltage sharing (OVS) is achieved, then, V_{o1}=V_{o2}=…=V_{on}. Substituting this result for OVS into (1), gives:

$$I_{in1} = I_{in2} = ... = I_{inn} \tag{2}$$

It should be noted that input current sharing (ICS) is automatically achieved as long as OVS is achieved. Alternatively, if all modules share the same input current, then output voltage sharing is also achieved. In this study, OVS is applied to achieve power balancing.

The small-signal equivalent circuit of two IPOS connected PS-FB converters, shown in Fig.3, is given as an example, where k_1 and k_2 are the transformer turn ratios, L_r is the transformer leakage inductance, D_e is effective duty ratio per module [7], L_{f1}, L_{f2}, C_{f1} and C_{f2} are filter inductances and capacitances for modules 1 and 2 respectively, input voltage perturbation is represented by Δv_{in}, input current perturbations for the two modules are Δi_{in1} and Δi_{in2} respectively, filter inductor current and capacitor voltage perturbations are represented by Δi_{lf1}, Δi_{lf2}, Δv_{o1}, Δv_{o2} respectively, Δd_1 and Δd_2 are duty ratio perturbations, and Δd_{v1}, Δd_{v2}, Δd_{i1} and Δd_{i2} respectively represent duty ratio perturbations due to input voltage and output current, and are defined in (3) [7].

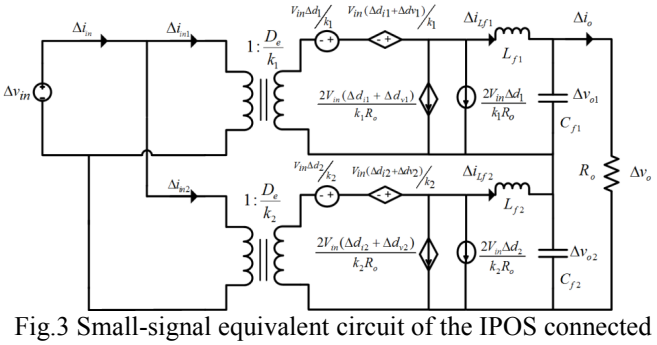


Fig.3 Small-signal equivalent circuit of the IPOS connected two-module system

$$\begin{cases} \Delta d_{v1} = \dfrac{8L_r D_e f_s}{k^2 V_{in} R_o} \Delta v_{in} \\ \Delta d_{v2} = \dfrac{8L_r D_e f_s}{k^2 V_{in} R_o} \Delta v_{in} \\ \Delta d_{i1} = -\dfrac{4L_r f_s}{k V_{in}} \Delta i_{lf1} \\ \Delta d_{i2} = -\dfrac{4L_r f_s}{k V_{in}} \Delta i_{lf2} \end{cases} \tag{3}$$

It is assumed that two modules have the same effective duty ratio, transformer turns ratios, and capacitor and inductor values, i.e. $k_1=k_2=k$, $L_{f1}=L_{f2}=L_f$, $C_{f1}=C_{f2}=C_f$, and $C_{d1}=C_{d2}=C_d$. From Fig.3, equations (4) can be obtained:

$$\begin{cases} \dfrac{D_e \Delta v_{in}}{k} + \dfrac{\mathrm{V}_{in}}{k}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1}\right) = s\mathrm{L}_f \Delta i_{lf1} + \Delta v_{o1} \\ \dfrac{D_e \Delta v_{in}}{k} + \dfrac{\mathrm{V}_{in}}{k}\left(\Delta d_2 + \Delta d_{v2} + \Delta d_{i2}\right) = s\mathrm{L}_f \Delta i_{lf2} + \Delta v_{o2} \\ \dfrac{k}{D_e}\Delta i_{in1} = \dfrac{2\mathrm{V}_{in}}{kR_o}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1}\right) + \Delta i_{lf1} \\ \dfrac{k}{D_e}\Delta i_{in2} = \dfrac{2\mathrm{V}_{in}}{kR_o}\left(\Delta d_2 + \Delta d_{v2} + \Delta d_{i2}\right) + \Delta i_{lf2} \end{cases} \tag{4}$$

Module voltage perturbations can be obtained as (5):

$$\begin{cases} \Delta v_{o1} = \dfrac{1}{sC_f}\left[\Delta i_{lf1} - \dfrac{\left(\Delta v_{o1} + \Delta v_{o2}\right)}{R_o}\right] \\ \Delta v_{o2} = \dfrac{1}{sC_f}\left[\Delta i_{lf2} - \dfrac{\left(\Delta v_{o1} + \Delta v_{o2}\right)}{R_o}\right] \end{cases} \tag{5}$$

which can be rewritten as (6):

$$\begin{cases} \Delta v_{o1} = \dfrac{1+sC_f R_o}{s^2 C_f{}^2 R_o + 2sC_f} \Delta i_{lf1} - \dfrac{1}{s^2 C_f{}^2 R_o + 2sC_f} \Delta i_{lf2} \\ \Delta v_{o2} = -\dfrac{1}{s^2 C_f{}^2 R_o + 2sC_f} \Delta i_{lf1} + \dfrac{1+sC_f R_o}{s^2 C_f{}^2 R_o + 2sC_f} \Delta i_{lf2} \end{cases} \tag{6}$$

Based on (6), the transfer function between module voltages and currents can be obtained in matrix form (7):

$$\begin{bmatrix} \Delta v_{o1} \\ \Delta v_{o2} \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \begin{bmatrix} \Delta i_{lf1} \\ \Delta i_{lf2} \end{bmatrix} \tag{7}$$

where:

$$\begin{cases} G_{11} = G_{22} = \dfrac{1+sC_f R_o}{s^2 C_f{}^2 R_o + 2sC_f} \\ G_{12} = G_{21} = -\dfrac{1}{s^2 C_f{}^2 R_o + 2sC_f} \end{cases} \tag{8}$$

Addition of the first two equations in (4) gives:

$$\begin{aligned} &\frac{2D_e \Delta v_{in}}{k} + \frac{\mathrm{V}_{in}}{k}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1} + \Delta d_2 + \Delta d_{v2} + \Delta d_{i2}\right) = \\ &s\mathrm{L}_f \Delta i_{lf1} + \Delta v_{o1} + sL_f \Delta i_{lf2} + \Delta v_{o2} \end{aligned} \tag{9}$$

Assuming that $\Delta v_{in}=0$, and $\Delta d_k=0$ (k=1,2 and k≠j), and substituting (5) into (9), the relationship between load voltage and duty ratio is obtained as (10):

$$G_{ovd} = \frac{\Delta v_o}{\Delta d_j} = \frac{V_{in}/k}{L_f C_f s^2 + \left[\dfrac{2L_f}{R_o} + \dfrac{4L_r f_s}{k^2} C_f\right] s + \dfrac{8L_r f_s}{k^2 R_o} + 1} \tag{10}$$

From (10), the control-to-output current ratio can be obtained as (11), by assuming $\Delta v_{in}=0$, and $\Delta d_k=0$ (k=1,2 and k≠j):

$$\begin{aligned} G_{oi} &= \frac{\Delta i_o}{\Delta d_j} \\ &= \frac{V_{in}/k}{L_f C_f R_o s^2 + \left[2L_f + \dfrac{4L_r f_s R_o}{k^2} C_f\right] s + \dfrac{8L_r f_s}{k^2}} \end{aligned} \tag{11}$$

The load disturbance is measured by its effect on the load voltage, as shown in (12):

$$G_{ov} = \frac{\Delta v_o}{\Delta i_o} = \frac{2sL_f + \dfrac{8L_r f_s}{k^2}}{L_f C_f s^2 + \left[\dfrac{2L_f}{R_o} + \dfrac{4L_r f_s}{k^2} C_f\right] s + \dfrac{8L_r f_s}{k^2 R_o} + 1} \tag{12}$$

Substituting (3) and (6) into (4), assuming $\Delta v_{in}=0$, yields (13):

$$\begin{cases} \dfrac{\mathrm{V}_{in}}{k}\Delta d_1 = \left[\mathrm{L}_f s + \dfrac{1+C_f R_o s}{C_f{}^2 R_o s^2 + 2C_f s} + \dfrac{4L_r f_s}{k^2}\right] \Delta i_{lf1} - \dfrac{1}{C_f{}^2 R_o s^2 + 2C_f s} \Delta i_{lf2} \\ \dfrac{\mathrm{V}_{in}}{k}\Delta d_2 = -\dfrac{1}{C_f{}^2 R_o s^2 + 2C_f s} \Delta i_{lf1} + \left[\mathrm{L}_f s + \dfrac{1+C_f R_o s}{C_f{}^2 R_o s^2 + 2C_f s} + \dfrac{4L_r f_s}{k^2}\right] \Delta i_{lf2} \end{cases} \tag{13}$$

Rearranging (13), the relationship between duty ratio and inductor current can be represented as (14):

$$\begin{bmatrix} \Delta i_{lf1} \\ \Delta i_{lf2} \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} \Delta d_1 \\ \Delta d_2 \end{bmatrix} \tag{14}$$

where:

$$\begin{cases} g_{11} = g_{22} \\ = \dfrac{\mathrm{V}_{in}\left(s\mathrm{L}_f + \dfrac{1+sC_f R_o}{s^2 C_f{}^2 R_o + 2sC_f} + \dfrac{4L_r f_s}{k^2}\right)}{k\left(s\mathrm{L}_f + \dfrac{R_o}{s^2 C_f{}^2 R_o + 2sC_f} + \dfrac{4L_r f_s}{k^2}\right) \times \left(s\mathrm{L}_f + \dfrac{2+sC_f R_o}{s^2 C_f{}^2 R_o + 2sC_f} + \dfrac{4L_r f_s}{k^2}\right)} \\ g_{12} = g_{21} \\ = -\dfrac{\mathrm{V}_{in}\left(\dfrac{-1}{s^2 C_f{}^2 R_o + 2sC_f}\right)}{k\left(s\mathrm{L}_f + \dfrac{R_o}{s^2 C_f{}^2 R_o + 2sC_f} + \dfrac{4L_r f_s}{k^2}\right) \times \left(s\mathrm{L}_f + \dfrac{2+sC_f R_o}{s^2 C_f{}^2 R_o + 2sC_f} + \dfrac{4L_r f_s}{k^2}\right)} \end{cases} \tag{15}$$

Hence, the transfer function between module output voltage and duty ratio is given by:

$$\begin{bmatrix}\Delta v_{o1}\\ \Delta v_{o2}\end{bmatrix}=\begin{bmatrix}G_{11} & G_{12}\\ G_{21} & G_{22}\end{bmatrix}\begin{bmatrix}\Delta i_{lf1}\\ \Delta i_{lf2}\end{bmatrix}$$
$$=\begin{bmatrix}G_{11} & G_{12}\\ G_{21} & G_{22}\end{bmatrix}\begin{bmatrix}g_{11} & g_{12}\\ g_{21} & g_{22}\end{bmatrix}\begin{bmatrix}\Delta d_1\\ \Delta d_2\end{bmatrix} \quad (16)$$
$$=\begin{bmatrix}G_{11}g_{11}+G_{12}g_{21} & G_{11}g_{12}+G_{12}g_{22}\\ G_{21}g_{11}+G_{22}g_{21} & G_{21}g_{12}+G_{22}g_{22}\end{bmatrix}\begin{bmatrix}\Delta d_1\\ \Delta d_2\end{bmatrix}$$

The transfer functions of the IPOS DC/DC converter derived in this section will be used in later to facilitate control design.

2.2 Lyapunov Closed-Loop Design for Output Voltage

From (10), the linear PI output voltage closed-loop controller is shown in Fig.4, and is based on a small-signal model which uses linearised large-signal state-space models around an equilibrium point to enable closed-loop design [8].

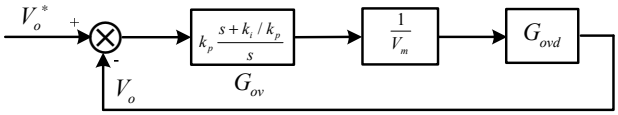


Fig.4 PI output voltage closed-loop controller

However, compared to a linear control technique such as PI control, some non-linear techniques can provide an improved transient response which is robust to load, input and parameter variations [9]. Most of the non-linear control laws are complex, which makes it difficult to apply, but the linearisation schemes have the advantage of reducing the converter model to an equivalent output filter model which significantly simplifies the robust control design process.

A linearised control scheme for a single DC/DC converter, and a novel reduced equivalent model of the IPOS DC/DC converter incorporating closed-loop output voltage control are presented in Fig.5 [10] and Fig.6 respectively. These provide a linear representation of converter behaviour under large-signal variation which is suitable for faster control response and estimation of the converter state variables.

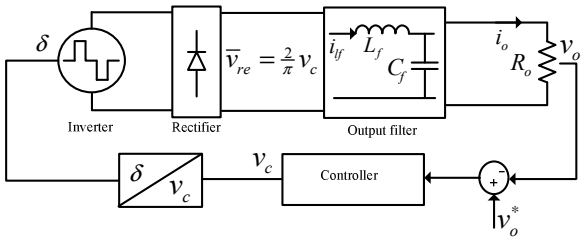


Fig.5 Closed-loop output voltage control configuration using the linearisation scheme

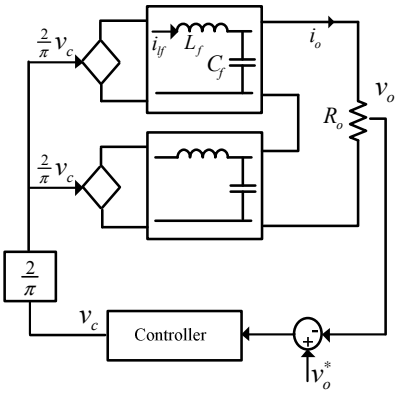


Fig.6 Equivalent model for the IPOS DC/DC converter

From Fig.6, and using (17) and (18), control variable v_c is expressed in a second order transfer function of the output voltage (19).

$$\frac{di_{lf}}{dt}=\frac{1}{L_f}\left(\frac{2}{\pi}v_c-\frac{1}{2}v_o\right) \quad (17)$$

$$\frac{dv_o}{dt}=\frac{2}{C_f}(i_{lf}-i_o)=\frac{2}{C_f}\left(i_{lf}-\frac{v_o}{R_o}\right) \quad (18)$$

which leads to

$$\ddot{v}_o=\frac{2}{C_f}\left(-\frac{v_o}{2L_f}+\frac{2v_c}{\pi L_f}-\frac{\dot{v}_o}{R_o}\right) \quad (19)$$

To control the IPOS DC/DC converter output voltage, the output voltage error signal (20) is required [10]:

$$e=v_o^*-v_o \quad (20)$$

In (21) it is assumed that $v(x)$ is the first order control Lyapunov function and that α is proportionality constant:

$$v=\frac{1}{2}(\dot{e}+\alpha e)^2 \quad (21)$$

According to Lyapunov's second condition, the derivative of v is negative, where β is a strictly positive proportionality constant.

$$\dot{v}=(\dot{e}+\alpha e)(\ddot{e}+\alpha\dot{e})=-\beta v<0 \quad (22)$$

$$(\ddot{e}+\alpha\dot{e})=-\frac{1}{2}\beta(\dot{e}+\alpha e) \quad (23)$$

Assuming v_o^* to be constant, $\dot{e}=-\dot{v}_o$, $\ddot{e}=-\ddot{v}_o$ and

$$\ddot{v}_o=\frac{\alpha\beta}{2}(v_o^*-v_o)-\frac{\beta}{2}\dot{v}_o-\alpha\dot{v}_o=\frac{2}{C_f}\left(\frac{2v_c}{L_f\pi}-\frac{v_o}{2L_f}-\frac{\dot{v}_o}{R_o}\right) \quad (24)$$

Substituting this result into (17) and (18) yields (25):

$$v_c=\frac{\alpha\beta C_f L_f\pi}{8}e+\frac{C_f L_f\pi}{4}\left(\frac{\beta}{2}+\alpha-\frac{2}{R_o C_f}\right)\dot{e}+\frac{\pi}{4}v_o \quad (25)$$

It can be seen from (25) that the first and second terms represent a PD controller and will eventually decay to 0 as the system converges to the output voltage reference value. v_o is a feed-forward term to speed start-up and to help stabilise the controller. Therefore, (25) can be rewritten as (26):

$$v_c = k_p e + k_d \dot{e} + \frac{\pi}{4} v_o \tag{26}$$

The transfer function between the output voltage and the adjusted output from the load voltage controller can be obtained from Fig.6:

$$G_{oc} = \frac{4}{\pi} \frac{1}{L_f C_f s^2 + 1} \tag{27}$$

Thus, the closed-loop output voltage controller obtained using the Lyapunov approach is shown in Fig.7.

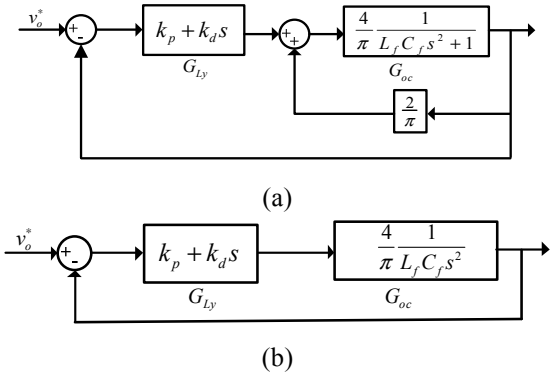


Fig.7 Closed-loop Lyapunov controller (a) full structure (b) reduced equivalent controller due to feed-forward scheme

Thus, the system open-loop, closed-loop and characteristic equation can be derived as (28-30):

$$G_{ol} = \frac{4}{\pi} \frac{k_p + k_d s}{L_f C_f s^2} \tag{28}$$

$$H_{cl} = \frac{4k_p + 4k_d s}{L_f C_f \pi s^2 + 4k_p + 4k_d s} \tag{29}$$

$$s^2 + \frac{4k_d}{L_f C_f \pi} s + \frac{4k_p}{L_f C_f \pi} = 0 \tag{30}$$

By designing the damping ratio and natural frequency from the system characteristic equation, the required closed-loop performance can be achieved. With the design specifications of 5% overshoot and 4ms settling time, the system root locus plot is given in Fig.8.

Fig.9 shows that the system bandwidth achieved using PI control is 1.29kHz, whilst that achieved using the Lyapunov controller is 2.39kHz and results in superior dynamic performance and disturbance rejection capability. Therefore, the control scheme requires one master module using Lyapunov control which produces the main control signal Δi (current command) to track the output voltage reference, and (n-1) slave modules which produce the voltage balancing current reference quantities Δi_i (i=1,2,…,n-1). In this case, $v_{o1}^* = v_{o2}^* = v_{o(n-1)}^* = V_o / n$. The sum of the current reference $\sum_{i=1}^{n-1} \Delta i_i$ produced by all of the slave modules is subtracted from the current reference for the master module, and Δi is added to the current reference of each slave module Δi_i (i=1,2,…,n-1). A third current control loop is added to guarantee current performance and the control scheme adjusts the system using individual inner current controllers, which are designed according to (14), for each module. The resulting control structure is shown in Fig.10.

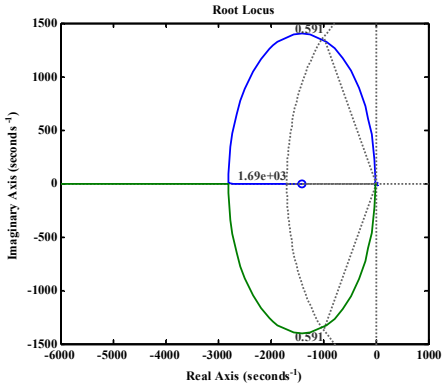


Fig.8 Root locus for system with Lyapunov controller

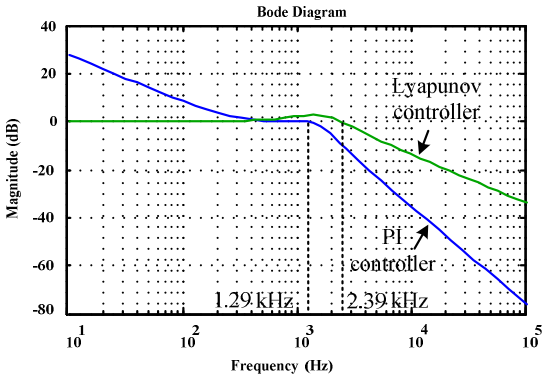


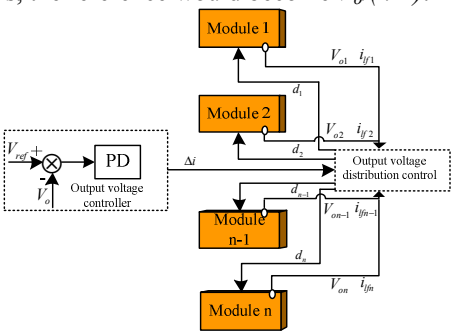
Fig.9 Closed-loop bandwidth

2.3 Fault Detection and Protection Issues

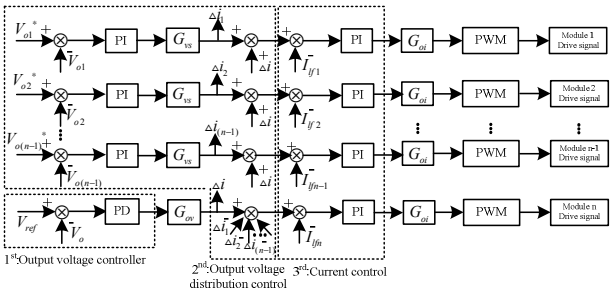
The multi-module DC/DC converter has internal fault management capability, in that faulty modules may be blocked in order to allow continued system operation without any performance degradation. Such a feature is normally achievable by incorporating redundant modules to allow re-configuration of the power circuit and bypassing of the faulty modules. The modularity feature allows (n+k) redundancy, where n is the number of modules required to ensure that each module operates within its voltage rating, and k is the number of redundant modules that can be used to replace k faulty modules and maintain an uninterrupted operation. (n+1) redundancy is introduced in this circuit.

The modular structure facilitates location of the faulty module. The failure of one module is, in this case, detected by

monitoring whether or not its output voltage and current fall outside predefined limits, e.g. voltage safety region $[0.2V_o<V_{oi}<0.3V_o]$ $(i=1,2,\ldots,4)$ for a 4-module converter. The faulty module is then isolated by blocking its front-end pulse width modulated H-bridge converter and bypassing its output diode bridge using a combination of a bypass switch and a bleed resistor to dissipate the energy stored in the filter capacitor. Any module can be operated in either an active state or a blocked state. If any slave unit fails, the system will locate the fault, block the faulty module and remain operational by simply changing the voltage reference to the slaves. For example, in a healthy n-module converter, the voltage reference for all slave modules is V_o/n, but if one module fails, the reference would become $V_o/(n\text{-}1)$.



(a)



(b)

Fig.10 (a) Output voltage Lyapunov control (b) Complete three loop control

The operation of the slaves is, however, dependent upon the master module control signals, i.e. if the master module malfunctions the overall system may fail [11]. In the previous case where a specific module is designated as 'master' under all conditions, the system will have a decreased reliability and modularity caused by a faulted master control module. In order to avoid system collapse, a 'non-dedicated master' approach is proposed, which enables the role of 'master' to be allocated to another healthy module in the event that the original master module fails. Because each module has the ability to becoming a master if required, any module may malfunction without further affecting the operation of the whole system.

Detailed description of the control is given as follows. For an n-module converter, the system assigns each module with a specific numerical identifier (between 1 and n). The control system then assigns the status signal '0' to module '1', designating it as master, and status signal '1' to the remaining modules, thereby identifying them as the slaves. The fault detection and protection function is actived when a module's output voltage or current falls outside predefined limits. If the module with status signal '1', i.e. a slave module, fails the voltage reference for the slave modules is updated to $V_o/(n\text{-}1)$. The role of 'master' is fixed to the designated module. When a failure of the master module occurs, module '2' becomes the new master and the voltage reference for the slave modules is updated. Meanwhile, the system immediately isolates the faulted previous 'master' module. The failure flow graph for a 4-module converter is shown in Fig.11.

3 Simulation Results

In order to evaluate the proposed control scheme for the IPOS DC/DC converter, a system (shown in Fig.12) consisting of a generator, a fully-rated uncontrolled rectifier and an IPOS DC/DC converter with rated output power of 5MW, is simulated. Generator output voltage is 2500V at 50Hz, the high-frequency transformer operates at 5kHz and has a turns ratio of 2500:8250V, and the load voltage is maintained at 33kV. Module 1 is initially chosen as the master module. To test the effectiveness of the power balancing function, mismatches of +10% in transformer turns ratio of Module 1 and +10% in the output filter capacitor of Module 2 are introduced. Meanwhile, a permanent short-circuit fault is applied at the output terminals of Module 1 at t=50ms. Fig.13 presents selected simulation results.

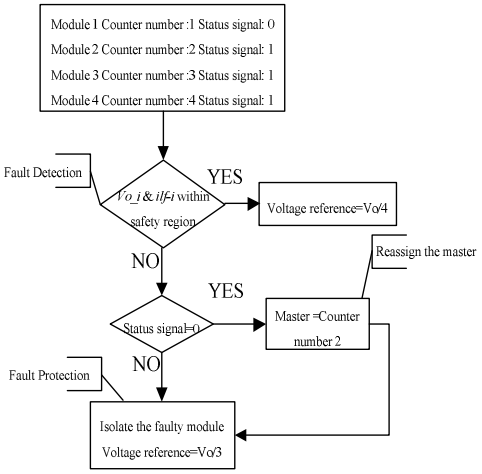


Fig.11 Flow chart for the 'non-dedicated master' control scheme

Fig.13(a) shows the converter output voltage v_o and Fig.13(b) shows the individual module output voltages (v_{o1}, v_{o2}, v_{o3} and v_{o4}). The results show that, before the fault, the proposed control scheme ensures output voltage balancing among the modules despite the mismatches in various module parameters. Following the fault at t=50ms, the faulty module is isolated and the output voltages of the remaining healthy modules are boosted to compensate the lost module. Output voltage v_o is maintained at its pre-fault value and is shared equally between the healthy modules. These results show that

the proposed control scheme manages failure of the master module, whilst ensuring continuous operation of and equal voltage sharing among the remaining healthy modules.

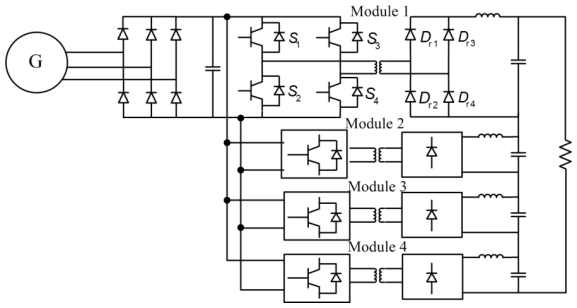


Fig.12 High-power system used in fault study

Following the fault, the 'non-dedicated master' control function reallocates the role of 'master' to a healthy module, which in this case is Module 2. This process is illustrated in Fig.13(c) which shows the signals that define 'master' and 'slave' status of the modules. The i^{th} module is defined as 'master' or 'slave' when d_i=0 or d_i=1 respectively. It can be seen that, following the fault, Module 1 is deselected as 'master' module and Module 2 is selected as the new 'master'.

4 Conclusions

A 'master-slave' control strategy for IPOS DC/DC converters facilitates power sharing with mismatched components among the modules is proposed. The previous fixed 'master-slave' scheme can respond appropriately to slave module faults only, necessitating development of an enhanced controller based on the concept of the 'non-dedicated master' that permits arbitrary reallocation of the role of 'master' to another healthy module. The system has been verified through simulation of a fully-rated wind turbine module and the proposed control strategy can be extended to converters composed from any number of modules. The results show that the system exploits true (n+1) redundancy in the event that the master module is faulted.

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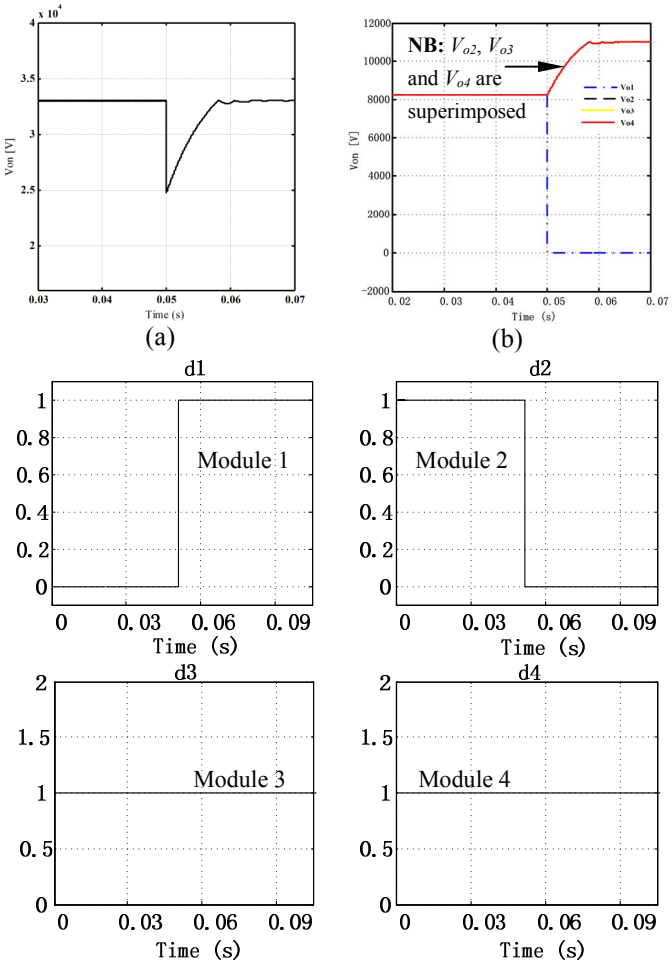

Fig.13 Response of (a) converter output voltage (b) module output voltage (c) allocation of 'master' and 'slave' roles

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