Submodule Configuration of HVDC-DC Auto Transformer Considering DC Fault

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Abstract: This paper studies the submodule configuration of MMC based non-isolated HVDC-DC autotransformer (HVDC-AT) with DC fault blocking capability, including two-terminal and multi-terminal topologies. The operation principle of the HVDC-AT is described. Considering the arm current differences, the total number of required semiconductors for the HVDC-AT is derived and is compared with the MMC based isolated front-to-front (F2F) DC transformer. A full operation process for the multi-terminal HVDC-AT considering DC fault is then presented, including normal operation, fault isolation and continuous operation of healthy converters after fault. The submodule configuration and fault recovery of the multi-terminal HVDC-AT are validated by simulations using PSCAD/EMTDC.

1. Introduction

Renewable energy is increasingly important nowadays due to the growing environmental concerns and attempts to reduce dependency on fossil fuels. Among the various renewable resources, offshore wind power is the most promising one in technical and economic terms. It has been widely accepted that HVDC technology is more attractive and likely to be the only feasible option for connecting large offshore wind farms over long distance [1, 2].

Due to different manufacturers and time of installation, the existing HVDC projects have a wide variety of DC voltage levels. For the first four HVDC connected offshore wind farms the DC voltage levels are all different (±150kV, ±250kV, ±300kV and ±320kV). Without DC/DC converters, these schemes can only be integrated into the DC grid by their AC connections [3].

As the conventional DC/DC topologies with low or medium voltage and power rating are not suitable for HVDC applications, many studies have been carried out on high-power high-voltage DC/DC converters for HVDC system [4-10].

Modular Multilevel Converter (MMC) is currently the optimal solution for HVDC applications due to its significant advantages over the conventional 2-level topology, e.g. modular design, scalability, low single device switching frequency, excellent harmonic performance, etc [11, 12]. Recently, MMC based high-power high-voltage DC/DC converters have been proposed [13-22]. An isolated front-to-front (F2F) configuration is presented in [13], where both MMCs contribute to the voltage elevation besides the AC transformer stage. However, the transformer is exposed to high dv/dt at the rising and falling edges of the square waveform AC link voltages. To avoid this problem, a quasi two-level (Q2L) DC/DC converter has been proposed in [14], where the converter generates a square wave with controllable dv/dt by employing the SM voltages to create transient intermediate voltage level. This significantly reduces the size of the SM capacitors compared to conventional MMC. Another F2F DC/DC converter is proposed in [15], where alternate arm converter (AAC) or MMC can be used. The use of higher inner AC frequency is discussed and the results show that an AC frequency of 350 Hz allows for significant saving in volume and acceptable increase in losses.

A non-isolated modular multilevel DC/DC converter with bidirectional fault blocking capability is presented in [16]. Different from the aforementioned F2F DC-AC-DC technology, the proposed DC/DC converter uses multiple interleaved strings of cascaded SMs to perform single-stage bidirectional DC/DC conversion. However, large magnetically coupled inductors are required for the DC/DC converter to filter out AC components from the DC side. The HVDC-DC autotransformer (HVDC-AT) is proposed in [18-20], which is also a single-stage converter consisting of two series-connected voltage source converters with a common AC link to transfer energy between the upper and the lower converters. The proposed HVDC-AT can be used to interconnect different DC transmission configurations and allows the asymmetrical operation of bipolar DC transmission configuration in the event of a converter failure or during a DC pole-to-pole fault [19]. In [20], the energy conversion efficiency of the proposed HVDC-AT

is studied and compared to the F2F configuration. The HVDC-AT with DC fault blocking capability is further analyzed and a family of possible HVDC-AT topologies are then proposed in [21].

The total number of required semiconductor devices for a two-terminal HVDC-AT with forward and reverse fault isolation capability (HBSMs in the lower converter and FBSMs+HBSMs in the upper converter) was compared with that of the F2F adopting HBSMs in both converter stations [18]. However, the difference in the arm currents of the two DC transformers was not considered. For instance, the converter station with arm current higher than the current capability of a single device requires parallel connection of multiple IGBTs. Therefore, to make a full comparison of the required semiconductor devices in the two DC transformers, the ratio between the total required device power capacity and the available single device capacity is considered in this paper.

For connecting DC networks with more than two DC voltage levels and catering for the need of network protection and power flow control, multi-terminal DC/DC converter is likely to be more cost effective and desirable [22-24].

A Q2L three-terminal DC/DC converter was proposed in [14]. When a fault occurs at any side of the DC grid, the fault can be isolated immediately by blocking all the three converters. A three-terminal DC/DC converter based on a simplified hybrid MMC configuration, proposed in [22], is able to block the faulty side terminal, while continue operating the other terminals connected to the healthy DC grids. However, the aforementioned multi-terminal DC/DC converters with isolation all require full DC-AC-DC energy conversions between the interconnected DC networks. By connecting the MMCs in series on the DC side, the electrical non-isolated multi-terminal HVDC-AT proposed in [24] significantly reduces the cost and operational power losses. However, DC fault was not considered for the SM configuration of each converter station.

System reliability of the multi-terminal HVDC-AT during failure of a converter station has been addressed in [24]. It claims that, to avoid over voltage of the healthy converters, more SMs need to be

added only during the failure of the converters connecting the medium voltage level DC grid. During a permanent DC pole-to-pole fault applied in the low voltage level DC grid, the voltage stress increases from the difference between the medium voltage level and low voltage level to the medium voltage level. Thus, to keep normal operation of the multi-terminal HVDC-AT after fault isolation, extra HBSMs are also required for the medium voltage converter to support higher DC voltage. Moreover, to enable immediate DC fault isolation, extra FBSMs need also to be added to the converter stations to block the DC fault current leading to further increase in the cost of the DC transformer.

In this paper, the total number of required semiconductor devices for the HVDC-AT, considering arm current difference, is derived and compared with that in the F2F configuration, including the two-terminal and multi-terminal DC transformers. The SM configuration of each converter considering DC fault is analyzed and a full operation process for the multi-terminal HVDC-AT is then presented, including normal operation, fault isolation and continuous operation of the healthy converters after the DC fault. The analysis is verified by a three-terminal DC test system in PSCAD/EMTDC.

2. Two-Terminal High Voltage DC Transformers with DC Fault Isolation Capability

For the two-terminal and the following multi-terminal F2F and HVDC-AT, the capacity of the semiconductors of each SM is assumed to be identical and is noted as P_{IGBT}. Taking the arm current difference into consideration, the total number of equivalent semiconductors for each DC transformer can be derived according to the ratio between the required total device capacity and single device capacity of P_{IGBT}.

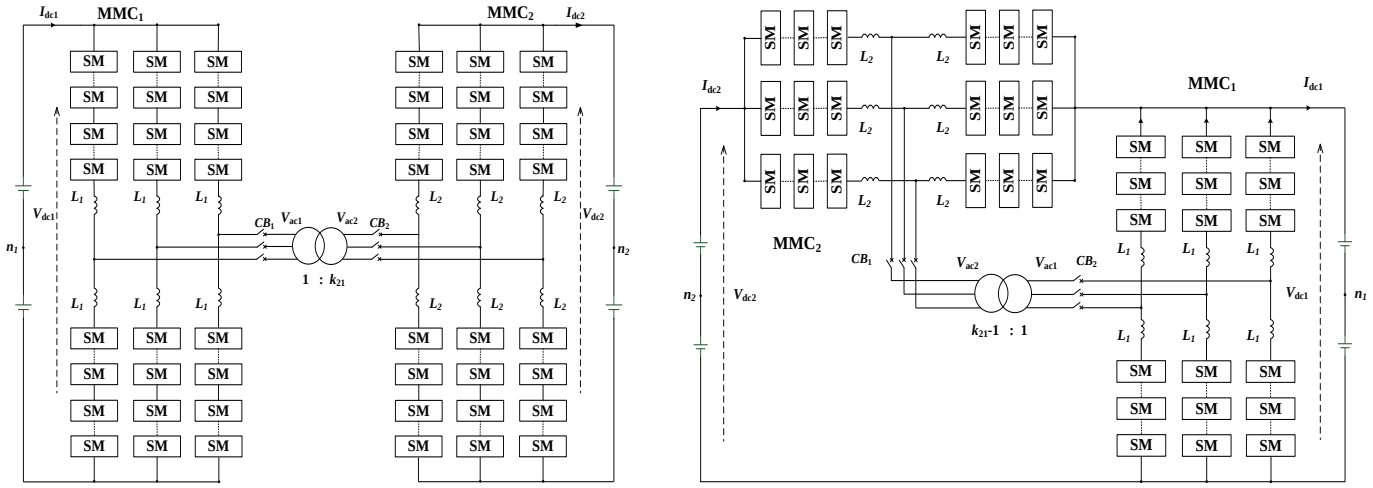
2.1. Front-to-Front HVDC-DC Transformer

As shown in Fig. 1a, the two-terminal F2F HVDC-DC transformer is composed of two MMCs, which are interconnected by a two-winding AC transformer. The two MMCs have the same topology and MMC_1 is taken as an example for illustration. Each arm has N HBSMs, V_{dc1} is the low DC link voltage, V_{ac1} is the low AC link line-to-line rms voltage, L_1 is the arm inductance, and V_c is the nominal SM

capacitor voltage. The ratio between the high DC link voltage V_{dc2} and low DC link voltage V_{dc1} is defined as as k_{21} (also the ratio between V_{ac2} and V_{ac1}). The total number of equivalent semiconductors for the F2F configuration is given by the sum of the semiconductors of both converter stations (all the semiconductor number calculations carried out in this paper are based on per arm value, and redundant SMs are not considered):

$$N_{F2F} = \frac{2NV_c i_{MMC1p}}{P_{IGBT}} + \frac{2k_{21}NV_c i_{MMC2p}}{P_{IGBT}} = \frac{2\sqrt{6}V_{dc1} + 4V_{ac1}}{3V_{ac1}P_{IGBT}} P_{max} \quad (1)$$

where i_{MMC1p} and i_{MMC2p} are the respective nominal peak arm currents of MMC_1 and MMC_2, P_{max} is the maximum active power exchange between the two DC grids.



a *b*

Fig. 1. Two-terminal MMC based DC transformer configurations
a Topology of F2F HVDC-DC transformer
b Topology of HVDC-DC auto transformer

Defining $(\sqrt{6}V_{dc1}+2V_{ac1})/3V_{ac1}P_{IGBT}$ as m, (1) can be rewritten as

$$N_{F2F} = 2mP_{max}. \quad (2)$$

When a DC pole-to-pole fault occurs at any side of the DC grid, the fault can be isolated immediately by blocking both converter stations. Therefore, no additional SMs are required to block DC fault.

2.2. HVDC-DC Auto Transformer

Different to the two-stage F2F configuration, the HVDC-AT shown in Fig. 1b is a single-stage DC transformer, where the sum of the DC voltages of MMC_1 and MMC_2 forms the high DC link voltage V_{dc2} and MMC_1 supports the low DC link voltage V_{dc1}.

The DC voltages and currents of each MMC are given by

$$\begin{cases} V_{MMC_2} = \dfrac{k_{21}-1}{k_{21}} V_{dc2} \\ V_{MMC_1} = \dfrac{1}{k_{21}} V_{dc2} \end{cases} \tag{3}$$

$$\begin{cases} I_{dc2} = \dfrac{P}{V_{dc2}} \\ I_{dc1} = (k_{21}-1)\dfrac{P}{V_{dc2}} \end{cases} \tag{4}$$

where P is the active power exchange between the two DC grids. Based on (3) and (4), the active power transferring through the AC link and the direct electrical connection are derived as

$$\begin{cases} P_{DC-AC-DC} = V_{MMC_2} I_{dc2} = \dfrac{k_{21}-1}{k_{21}} P \\ P_{direct} = V_{MMC_1} I_{dc2} = \dfrac{1}{k_{21}} P \end{cases}. \tag{5}$$

Assuming the ratio between V_{ac2} and V_{ac1} is (k_{21}-1) ($k_{21} > 1$), the total number of required equivalent semiconductors for the HVDC-AT is given by

$$N_{AT} = \frac{2(k_{21}-1)NV_c i_{MMC2p}}{P_{IGBT}} + \frac{2NV_c i_{MMC1p}}{P_{IGBT}} = \frac{(k_{21}-1)}{k_{21}} 2mP_{\max} \tag{6}$$

Comparing (6) to (2), the total number of equivalent semiconductors for the HVDC-AT, considering normal operation, is significantly reduced for a low or medium voltage elevation. For instance, when k_{21} equals 2, only half of the semiconductors will be needed for the HVDC-AT compared with the F2F. However, different from the F2F configuration which is capable of blocking DC fault without additional SMs, the HVDC-AT is a non-isolated configuration in which the fault current can feed into the faulty DC

grid due to the direct electrical connection. With a DC pole-to-pole fault applied at the high voltage DC grid , extra FBSMs are required for MMC_2 in order to ensure DC fault isolation, whereas MMC_1 can still be composed of HBSMs. Thus, the DC fault can be isolated following the blocking of MMC_2, if the series-connected voltage of the additional FBSMs, which are inserted into the fault current path, is higher than the low DC link voltage V_{dc1} [21]. The number of minimum FBSMs per arm added to MMC_2 is then obtained as

$$N_{FBSM} = \frac{V_{dc1}}{2V_c} = \frac{N}{2}. \tag{7}$$

When a DC pole-to-pole fault occurs at the low voltage DC grid, extra HBSMs is also required for MMC_2 to ensure forward DC fault isolation, and the DC voltage of MMC_2 has to meet the following requirement [21]

$$2V_{MMC_2} \geq V_{dc2}. \tag{8}$$

From (3) and (8), the minimum DC voltage ratio to provide inherent blocking capability (without extra HBSMs) during the DC pole-to-pole fault on low voltage side is derived as:

$$k_{21} \geq 2. \tag{9}$$

When the DC voltage ratio is higher than 2, by replacing HBSMs of the MMC_2 with an equal number of FBSMs, the total equivalent semiconductors (the number of semiconductors for one FBSM equals that of two HBSMs) of the HVDC-AT can be derived as

$$N_{AT} = \underbrace{\frac{2((k_{21}-1)N - \frac{1}{2}N + N)V_c i_{MMC2p}}{P_{IGBT}}}_{MMC_2} + \underbrace{\frac{2NV_c i_{MMC1p}}{P_{IGBT}}}_{MMC_1} = \frac{4k_{21}-3}{2k_{21}} m P_{\max}. \tag{10}$$

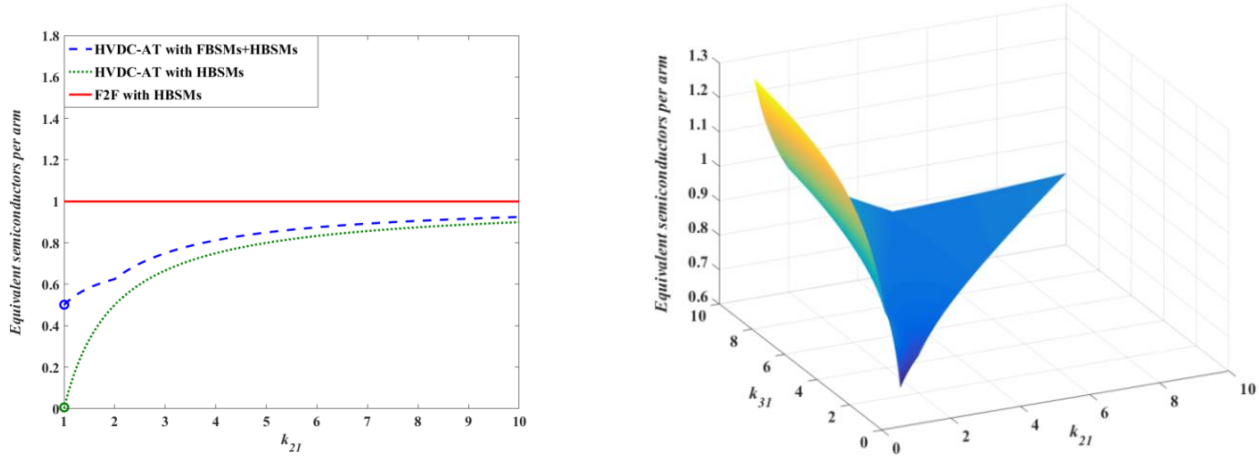
When the DC voltage ratio is less than 2, besides additional FBSMs according to (7), extra HBSMs are also required for MMC_2 in case DC fault occurs at low voltage DC grid [21]. The number of extra HBSMs per arm added to MMC_2 is given by

$$N_{addHBSM} = \frac{V_{dc2} - 2V_{MMC_2}}{2V_c} = (1 - \frac{k_{21}}{2})N. \tag{11}$$

The total number of equivalent semiconductors for the HVDC-AT is then derived as

$$N_{AT} = \underbrace{\frac{2((k_{21}-1)N + (1-\frac{k_{21}}{2})N - \frac{1}{2}N + N)V_c i_{MMC2p}}{P_{IGBT}}}_{MMC_2} + \underbrace{\frac{2NV_c i_{MMC1p}}{P_{IGBT}}}_{MMC_1} = \frac{3k_{21}-1}{2k_{21}} m P_{max}. \tag{12}$$

Fig. 2a compares the number of equivalent semiconductors per arm with the variation of the DC voltage ratio k_{21} for different DC transformer configurations, where the number of semiconductor is normalized by $2mP_{\max}$.



a *b*

Fig. 2. Equivalent semiconductor number for different DC transformer configurations
a Relationship of two-terminal HVDC-AT equivalent semiconductors per arm and DC voltage ratio k_{21} for different DC transformer configuration
b Relationship of three-terminal HVDC-AT equivalent semiconductors per arm for different DC voltage ratio k_{21} and k_{31}

As shown in Fig. 2a, more semiconductors are required for the F2F in the entire range of the DC voltage ratio. With k_{21} closing to unity, the number of equivalent semiconductors for the HVDC-AT without DC fault blocking capability (i.e. with only HBSMs) is nearly zero in theory, due to the near zero current in MMC_1 and near zero voltage on MMC_2 . The number of equivalent semiconductors for the HVDC-AT with DC fault blocking capability (i.e. with FBSMs and HBSMs) is only half of that of the F2F,

yielding lower capital cost and power losses. However, the difference in equivalent semiconductors between the two configurations gradually becomes smaller with the increase of the DC voltage ratio.

Compared with the F2F configuration, the capacity of the internal AC transformer for the HVDC-AT is reduced from full power rating to $P_{\text{DC-AC-DC}}$, according to (5). For instance, when k_{21} equals 2, only half of the capacity will be required for the internal AC transformer of the HVDC-AT. However, the internal AC transformer has a DC offset during normal operation of

$$V_{Tdcbias} = \frac{V_{dc2}}{2}. \tag{13}$$

Thus, although the required semiconductors and the internal AC transformer capacity of the HVDC-AT are reduced, the AC transformer has to be designed to cope with this DC offset especially when a high voltage elevation is required.

3. Multi-Terminal High Voltage DC Transformers with DC Fault Isolation Capability

3.1. Multi-Terminal Front-to-Front HVDC-DC Transformer

A multi-terminal DC transformer might be required for interconnecting DC grids with more than two DC voltage levels. Taking the three-terminal F2F HVDC-DC transformer as an example, it is consisted of three MMCs interconnected by a three-winding AC transformer, as illustrated in Fig. 3a, where V_{dc1}(V_{ac1}), V_{dc2}(V_{ac2}) and V_{dc3}(V_{ac3}) are the respective low, medium and high DC (AC) link voltages. The relationships of the DC (AC) link voltages are expressed as

$$\begin{cases} V_{dc1} = \dfrac{1}{k_{21}} V_{dc2} = \dfrac{1}{k_{21}k_{32}} V_{dc3} = \dfrac{1}{k_{31}} V_{dc3} \\ V_{ac1} = \dfrac{1}{k_{21}} V_{ac2} = \dfrac{1}{k_{21}k_{32}} V_{ac3} = \dfrac{1}{k_{31}} V_{ac3} \end{cases} \tag{14}$$

where k_{21} is the ratio between V_{dc2} and V_{dc1}(also the ratio between V_{ac2} and V_{ac1}), k_{31} is the ratio between V_{dc3} and V_{dc1}(also the ratio between V_{ac3} and V_{ac1}), and k_{32} is the ratio between V_{dc3} and V_{dc2} (also the ratio between V_{ac3} and V_{ac2}).

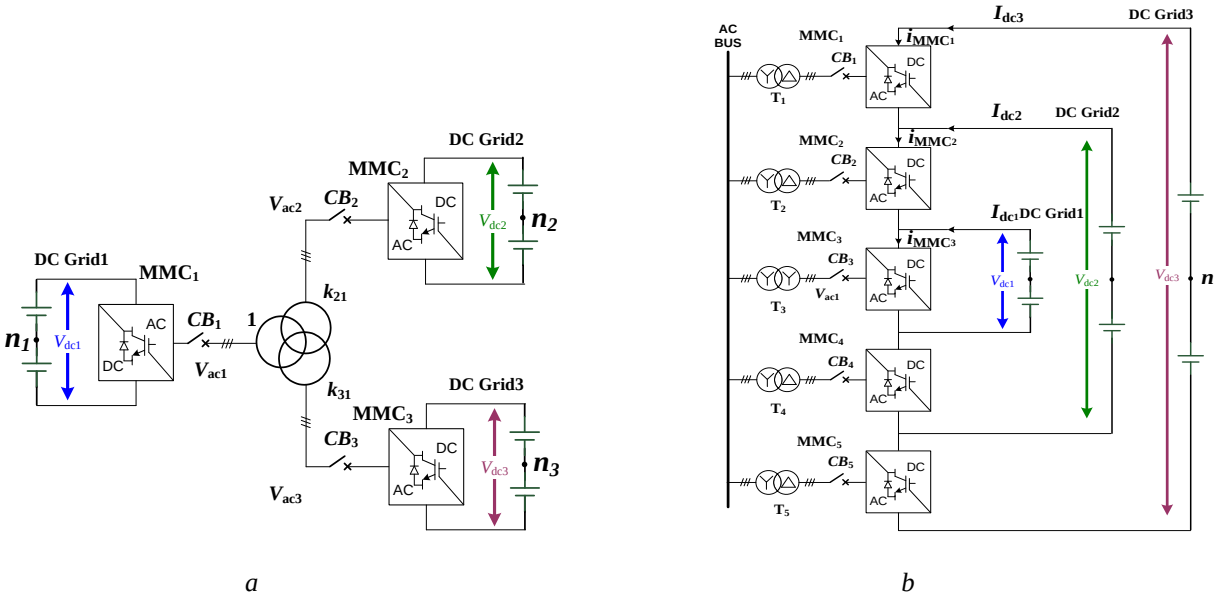


Fig. 3. Different three-terminal MMC based DC transformer configurations
a Topology of F2F HVDC-DC transformer
b Topology of HVDC-DC auto transformer

When a DC pole-to-pole fault occurs at any side of the DC network, the fault can be isolated immediately once all the converter stations are blocked. This leads to the temporary shutdown of all the terminals. After opening the AC breaker on the converter connecting to the faulty DC grid, the active power transmission between the other two healthy terminals can be resumed. Thus, no additional SMs are required to block DC fault and the total number of equivalent semiconductors for the three-terminal F2F DC transformer is given by the sum of the HBSMs of all the converter stations:

$$N_{F2F} = m(P_{1\max} + P_{2\max} + P_{3\max}) \tag{15}$$

where P_{1max}, P_{2max} and P_{3max} are the respective maximum active power exchanges between the three DC grids.

3.2. Multi-Terminal HVDC-DC Auto Transformer

Fig. 3b presents a three-terminal HVDC-AT, which consists of five series-connected MMCs with an AC common bus to transfer energy (DC/AC/DC) among the interconnected three DC grids [24]. The series connection of MMC_1~MMC_5 produces the high DC link voltage and the sum of MMC_2~MMC_4

forms the medium DC link voltage. MMC_3 supports the low DC link voltage. Due to the symmetry characteristics of the HVDC-AT topology, the DC voltages of each MMC can be expressed as

$$\begin{cases} V_{MMC_3} = V_{dc1} \\ V_{MMC_{2,4}} = \dfrac{V_{dc2} - V_{dc1}}{2} \\ V_{MMC_{1,5}} = \dfrac{V_{dc3} - V_{dc2}}{2} \end{cases}. \tag{16}$$

According to the positive direction shown in Fig. 3b, the DC currents flowing through each MMC can be derived as

$$\begin{cases} I_{dc1} = \dfrac{P_3}{k_{31}V_{dc1}} \\ I_{dc2} = \dfrac{P_2}{k_{21}V_{dc1}} + \dfrac{P_3}{k_{31}V_{dc1}} \\ I_{dc3} = \dfrac{P_1}{V_{dc1}} + \dfrac{P_2}{k_{21}V_{dc1}} + \dfrac{P_3}{k_{31}V_{dc1}} \end{cases} \tag{17}$$

where P_1, P_2, P_3 are the imported active power through the three DC links during normal operation, respectively.

Based on the direct power flow analysis method [24], the energy transfers through the AC links can be expressed as

$$\begin{cases} P_{MMC1} = \dfrac{k_{31} - k_{21}}{2k_{31}} P_3 \\ P_{MMC2} = \dfrac{(k_{21} - 1)(k_{31}P_2 + k_{21}P_3)}{2k_{21}k_{31}} \\ P_{MMC3} = P_1 + \dfrac{P_2}{k_{21}} + \dfrac{P_3}{k_{31}} \end{cases}. \tag{18}$$

With the same modulation index, the AC link line-to-line rms voltages of MMC_1~MMC_3 are (k_{31}-k_{21})V_{ac1}/2, (k_{21}-1)V_{ac1}/2, and V_{ac1}, respectively. According to (17) and (18), the nominal peak arm currents of each MMC can be derived as

$$\begin{cases} i_{MMC1p} = \left| \dfrac{\sqrt{6}V_{dc1} + 2V_{ac1}}{6k_{31}V_{dc1}V_{ac1}} P_3 \right|_{\max} \\ i_{MMC2p} = \left| \dfrac{\sqrt{6}V_{dc1} + 2V_{ac1}}{6k_{21}V_{dc1}V_{ac1}} P_2 + \dfrac{\sqrt{6}V_{dc1} + 2V_{ac1}}{6k_{31}V_{dc1}V_{ac1}} P_3 \right|_{\max} \\ i_{MMC3p} = \left| \dfrac{\sqrt{6}V_{dc1} + 2V_{ac1}}{6V_{dc1}V_{ac1}} P_1 + \dfrac{\sqrt{6}V_{dc1} + 2V_{ac1}}{6k_{21}V_{dc1}V_{ac1}} P_2 + \dfrac{\sqrt{6}V_{dc1} + 2V_{ac1}}{6k_{31}V_{dc1}V_{ac1}} P_3 \right|_{\max} \end{cases} . \tag{19}$$

Considering normal operation, the total number of equivalent semiconductors for the three-terminal HVDC-AT is

$$\begin{aligned} N_{AT} &= \frac{2}{P_{IGBT}}((k_{31} - k_{21})V_{dc1}i_{MMC1p} + (k_{21} - 1)V_{dc1}i_{MMC2p} + V_{dc1}i_{MMC3p}) \\ &= m\left(\left|\frac{k_{31} - k_{21}}{k_{31}} P_3\right|_{\max} + \left|\frac{k_{21} - 1}{k_{21}} P_2 + \frac{k_{21} - 1}{k_{31}} P_3\right|_{\max} + \left|P_1 + \frac{P_2}{k_{21}} + \frac{P_3}{k_{31}}\right|_{\max}\right). \end{aligned} \tag{20}$$

When a DC pole-to-pole fault occurs at any side of the DC network, the primary task is to isolate the fault. Similar analysis method as (7) ~ (12) can be adopted considering forward and reverse blocking capability of the converter stations. With MMC_3 composed of only HBSMs, the SM configuration of each MMC can then be derived as

$$N_{MMC2,4} = \begin{cases} \underbrace{\dfrac{2k_{21} - 3}{4}N}_{HBSM} + \underbrace{\dfrac{1}{4}N}_{FBSM} & k_{21} \geq 2 \\ \underbrace{\dfrac{k_{21} - 1}{4}N}_{HBSM} + \underbrace{\dfrac{1}{4}N}_{FBSM} & k_{21} < 2 \end{cases} \tag{21}$$

$$N_{MMC1,5} = \begin{cases} \underbrace{\dfrac{2k_{31} - 3k_{21}}{4}N}_{HBSM} + \underbrace{\dfrac{k_{21}}{4}N}_{FBSM} & k_{32} \geq 2 \\ \underbrace{\dfrac{k_{31} - k_{21}}{4}N}_{HBSM} + \underbrace{\dfrac{k_{21}}{4}N}_{FBSM} & k_{32} < 2 \end{cases} . \tag{22}$$

Considering fault isolation, the total number of equivalent semiconductors for the three-terminal HVDC-AT can then be derived as

$$N_{AT}=\begin{cases} m\left(\left|\frac{2k_{31}-k_{21}}{2k_{31}}P_3\right|_{\max}+\left|\frac{2k_{21}-1}{2k_{21}}P_2+\frac{2k_{21}-1}{2k_{31}}P_3\right|_{\max}+\left|P_1+\frac{P_2}{k_{21}}+\frac{P_3}{k_{31}}\right|_{\max}\right) & k_{32}\geq 2\ \ k_{21}\geq 2 \\ m\left(\left|\frac{2k_{31}-k_{21}}{2k_{31}}P_3\right|_{\max}+\left|\frac{k_{21}+1}{2k_{21}}P_2+\frac{k_{21}+1}{2k_{31}}P_3\right|_{\max}+\left|P_1+\frac{P_2}{k_{21}}+\frac{P_3}{k_{31}}\right|_{\max}\right) & k_{32}\geq 2\ \ k_{21}<2 \\ m\left(\left|\frac{k_{31}+k_{21}}{2k_{31}}P_3\right|_{\max}+\left|\frac{2k_{21}-1}{2k_{21}}P_2+\frac{2k_{21}-1}{2k_{31}}P_3\right|_{\max}+\left|P_1+\frac{P_2}{k_{21}}+\frac{P_3}{k_{31}}\right|_{\max}\right) & k_{32}<2\ \ k_{21}\geq 2 \\ m\left(\left|\frac{k_{31}+k_{21}}{2k_{31}}P_3\right|_{\max}+\left|\frac{k_{21}+1}{2k_{21}}P_2+\frac{k_{21}+1}{2k_{31}}P_3\right|_{\max}+\left|P_1+\frac{P_2}{k_{21}}+\frac{P_3}{k_{31}}\right|_{\max}\right) & k_{32}<2\ \ k_{21}<2 \end{cases}. \quad (23)$$

Assuming the maximum active power exchange among the DC Grid1~3 being 500MW, 1000MW, and 1500MW respectively, the required equivalent semiconductors per arm for the three-terminal HVDC-AT under different DC voltage ratios k_{21} and k_{31} with DC fault blocking capability can be calculated using (23) and is shown in Fig. 2b. The number of equivalent semiconductors for the HVDC-AT is normalized by the number of equivalent semiconductors for the three-terminal F2F given in (15). It can be seen that at certain voltage ratio, the three-terminal HVDC-AT requires more semiconductors than the F2F. For instance, the equivalent semiconductor number for the three-terminal HVDC-AT is 1.25 times that of F2F with k_{21} and k_{31} being 1.25 and 5.76 respectively under the above power ratings.

After DC fault isolation, to maintain continuous operation of other terminals connected to the healthy DC grids, the number of required semiconductors needs to be further increased. For instance, when a DC pole-to-pole fault occurs at DC Grid1 as shown in Fig. 4a, the fault can be isolated following the blocking of all the converters with the SMs configured according to (21)~(22). To maintain continuous active power exchange between DC Grid2 and DC Grid3 after fault isolation, the DC side of MMC_3 has to be bypassed as shown in Fig. 4a and $MMC_{1,\,2,\,4,\,5}$ can then be restarted. However, the DC voltages of $MMC_{2,\,4}$ will increase from $(V_{dc2}\text{-}V_{dc1})/2$ to $V_{dc2}/2$. Similarly, the DC voltages of $MMC_{1,\,5}$ will change from $(V_{dc3}\text{-}V_{dc2})/2$ to $(V_{dc3}\text{-}V_{dc1})/2$ if a DC pole-to-pole fault occurs at DC Grid2 as shown in Fig. 4b. Therefore, redundant HBSMs have to be added to prevent over voltage of the healthy converters after the fault.

Based on the above analysis, with MMC_3 formed by HBSMs, the SM configuration of each MMC to maintain continuous operation after fault can then be derived as

$$\begin{cases} N_{MMC_{2,4}} = \underbrace{\frac{2k_{21}-1}{4}N}_{HBSM} + \underbrace{\frac{1}{4}N}_{FBSM} & k_{31} \geq 2 \\ N_{MMC_{1,5}} = \underbrace{\frac{2k_{31}-k_{21}-2}{4}N}_{HBSM} + \underbrace{\frac{1}{4}N}_{FBSM} \end{cases} \tag{24}$$

$$\begin{cases} N_{MMC_{2,4}} = \underbrace{\frac{2k_{21}-1}{4}N}_{HBSM} + \underbrace{\frac{1}{4}N}_{FBSM} & k_{31} < 2 \\ N_{MMC_{1,5}} = \underbrace{\frac{k_{31}-k_{21}}{4}N}_{HBSM} + \underbrace{\frac{1}{4}N}_{FBSM} \end{cases} . \tag{25}$$

Different from the previous equivalent semiconductor calculation for fault isolation using the nominal peak arm current, the redundant equivalent semiconductors to keep continuous operation of the healthy side converters should be calculated using the peak arm current after fault recovery. Thus, the total equivalent semiconductors will be further increased considering continuous operation after the DC fault.

Compared with the multi-terminal F2F configuration, the AC transformers of the multi-terminal HVDC-AT also suffers DC bias voltages during normal operation, as depicted by (26):

$$\begin{cases} V_{T2dcbias} = (\frac{1+k_{21}}{4})V_{dc1} \\ V_{T1dcbias} = (\frac{k_{21}+k_{31}}{4})V_{dc1} \end{cases} \tag{26}$$

The DC bias voltages of the AC transformers will also change considering DC pole-to-ground fault, which may further increase the insulation cost.

To maintain continuous operation of the healthy terminals after a permanent DC pole-to-pole fault, the following procedures should be adopted for the multi-terminal HVDC-AT:

1) After a DC fault is detected, blocking all the converter stations to isolate the fault;
2) Opening the AC breaker of the faulty converter station;
3) Isolating the faulty DC cable or overhead line;

4) Connecting the backup DC line to provide a DC current path for the healthy converter stations (not necessary if the fault occurs at high voltage side DC grid) ;

5) Restarting the healthy converter stations.

4. Continuous Operation of Multi-Terminal HVDC-AT after Fault

To minimise the impact of a DC fault, the active power exchange between the healthy DC grids should ideally remain unchanged after fault recovery. Different from the multi-terminal F2F configuration, where the healthy converter stations can maintain the original power exchange and keep the arm current within its nominal peak value, the healthy converter stations of the multi-terminal HVDC-AT may suffer over current. Therefore, the post-fault arm current of each healthy converter is analysed in this section.

As shown in Fig.4a, when a DC pole-to-pole occurs at DC Grid1, the DC currents flowing through each MMC can be derived as

$$\begin{cases} I'_{dc1} = -\dfrac{P_{2\max}}{k_{31}V_{dc1}} \\ I'_{dc2} = \dfrac{k_{31}-k_{21}}{k_{21}k_{31}}\dfrac{P_{2\max}}{V_{dc1}} \end{cases} \tag{27}$$

where $P_{1\max}$, $P_{2\max}$ and $P_{3\max}$ are the maximum active power exported from DC Grid1~3 respectively and for this illustration it assumes $P_{1\max} < P_{2\max} < P_{3\max}$. Based on (27), the active power flowing through the AC link is expressed as

$$P'_{MMC1} = -P'_{MMC2} = -\frac{k_{31}-k_{21}}{2k_{31}}P_{2\max}. \tag{28}$$

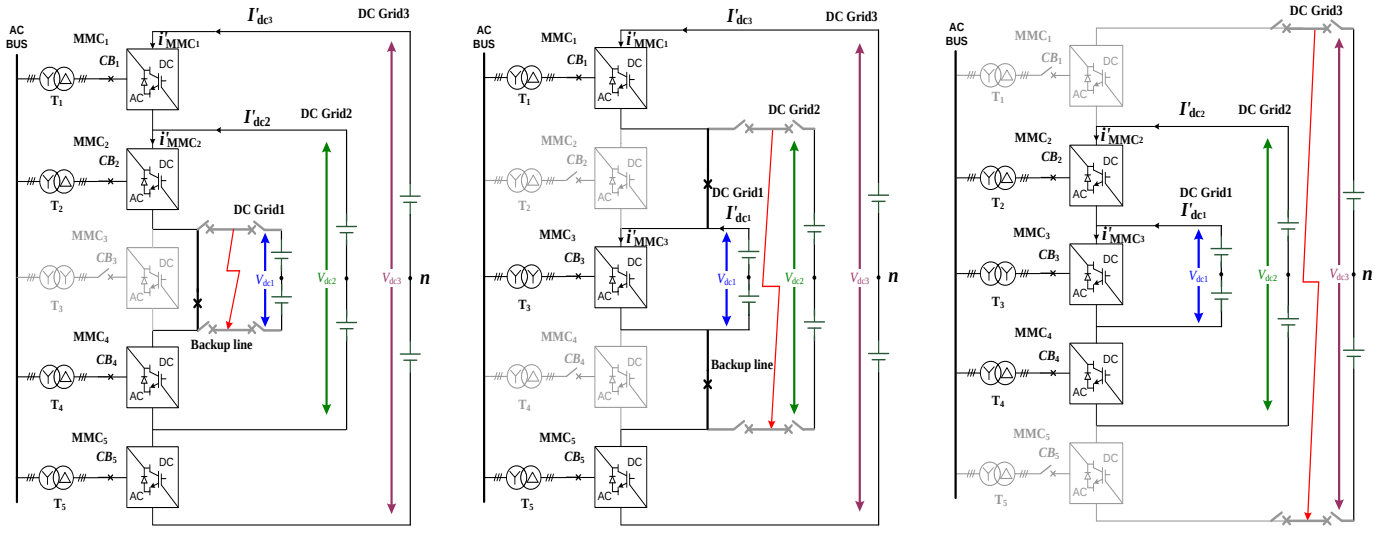


Fig. 4. Continuous operation after DC pole-to-pole fault
a Continuous operation after DC pole-to-pole fault on DC Grid1
b Continuous operation after DC pole-to-pole fault on DC Grid2
c Continuous operation after DC pole-to-pole fault on DC Grid3

From (27) and (28), the peak arm currents of each MMC after fault recovery can be derived as

$$\begin{cases} i'_{MMC1p} = \dfrac{\sqrt{6}V_{dc1} + 2V_{ac1}}{6k_{31}V_{dc1}V_{ac1}}P_{2\max} \\ i'_{MMC2p} = \dfrac{(k_{31}-k_{21})(\sqrt{6}k_{21}V_{dc1} + 2(k_{21}-1)V_{ac1})}{6k_{21}(k_{21}-1)k_{31}V_{dc1}V_{ac1}}P_{2\max} \end{cases}. \tag{29}$$

Similar analysis can be adopted when fault occurs at DC Grid2 and DC Grid3 shown in Figs. 4b and 4c, respectively. The peak arm currents of each MMC after fault recovery are

$$\begin{cases} i'_{MMC1p} = \dfrac{\sqrt{6}(k_{31}-1)V_{dc1} + 2(k_{31}-k_{21})V_{ac1}}{6k_{31}(k_{31}-k_{21})V_{dc1}V_{ac1}}P_{1\max} \\ i'_{MMC3p} = \dfrac{(k_{31}-1)(\sqrt{6}V_{dc1} + 2V_{ac1})}{6k_{31}V_{dc1}V_{ac1}}P_{1\max} \end{cases} \tag{30}$$

$$\begin{cases} i'_{MMC2p} = \dfrac{\sqrt{6}V_{dc1} + 2V_{ac1}}{6k_{21}V_{dc1}V_{ac1}}P_{1\max} \\ i'_{MMC3p} = \dfrac{(k_{21}-1)(\sqrt{6}V_{dc1} + 2V_{ac1})}{6k_{21}V_{dc1}V_{ac1}}P_{1\max} \end{cases}. \tag{31}$$

Table 1 Nominal parameters of the three-terminal HVDC-AT

Component	Value
SM nominal voltage	2kV
Number of SMs ($MMC_{1, 5}$)	60 FBSMs, 70 (40) HBSMs
Number of SMs ($MMC_{2, 4}$)	40 FBSMs, 20 (60) HBSMs
Number of SMs (MMC_3)	160 HBSMs
V_{dc1}/V_{ac1}	320kV/160kV
V_{dc2}/V_{ac2}	480kV/40kV
V_{dc3}/V_{ac3}	1000kV/130kV
$P_{1max}/ P_{2max}/ P_{3max}$	500MW/1000MW/1500MW

The three-terminal DC test system shown in Fig.5 is used as an example and its parameters are listed in Table 1. Considering fault isolation and continuous operation after fault, the SM configuration of each MMC can be calculated based on (21) ~ (22) and (24) ~ (25). Assuming P_{IGBT} equals 2.4MW (2000V/1200A), the total equivalent semiconductors for the three-terminal HVDC-AT and F2F are calculated as 2358 using (23) and 2875 using (15) respectively, indicating a 22% reduction for the HVDC-AT compared to F2F.

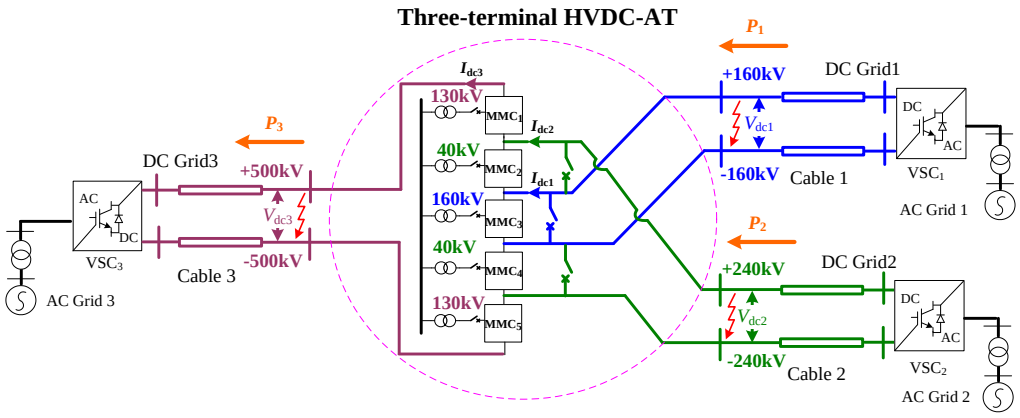


Fig. 5. **Three-terminal DC test system**

The capacity and peak arm current of each converter station after fault recovery are in Table 2 based on the previous analysis. As a comparison, the nominal capacity and peak arm current have also been calculated.

Table 2 Capacities and peak arm currents for the three-terminal HVDC-AT considering continuous operation after fault

$P_{MMC1,5}$	$P_{MMC2,4}$	P_{MMC3}	$i_{MMC1,5p}$	$i_{MMC2,4p}$	i_{MMC3p}
390MW	126.7MW	686.7MW	1.72kA	1.82kA	2.47kA
$P'_{MMC1,5}$	$P'_{MMC2,4}$	P'_{MMC3}	$i'_{MMC1,5p}$	$i'_{MMC2,4p}$	i'_{MMC3p}
260MW	260MW	-	1.15kA	3.01kA	-
170MW	-	340MW	0.70kA	-	1.22kA
-	83.3MW	166.7MW	-	1.20kA	0.60kA

As can be seen in Table 2, if a 1000MW active power exchange is maintained between DC Grid2 and DC Grid3 when a DC pole-to-pole fault occurs at DC Grid1, both MMC_2 and MMC_4 will be exposed to over current risk. The maximum active power exchange is derived according to (29) as 603MW (with peak arm current of $MMC_{1,5}$ and $MMC_{2,4}$ being 0.69kA and 1.82kA respectively). This implies that to maintain continuous operation of the multi-terminal HVDC-AT after fault, the active power exchange between the healthy DC grids might have to be reduced considering arm current limitation. In addition, to ensure maximum power exchange between the healthy grids, the capacity of the internal AC transformer for $MMC_{2,4}$ need to be increased from 126.7MW to 157MW, which may further increase the cost.

5. Simulation Results

To verify the SM configuration analysis and fault recovery of the multi-terminal HVDC-AT, the three-terminal DC test system shown in Fig. 5 is simulated using PSCAD/EMTDC. Average model is adopted for MMC_1~MMC_5 to accelerate the simulation speed [22], where the arms of each converter are modelled as controlled voltage sources formed by the FBSMs and HBSMs. The adopted average model can accurately represent the MMC behaviour under various operating conditions, including a pole-to-pole DC fault [22]. Each SM is rated at 2kV, the DC link voltages are 320kV, 480kV and 1000kV respectively. The AC bus of the HVDC-AT is controlled by MMC_1 at 160kV (line-to-line rms voltage), with a frequency of 50Hz. With only forward and reverse DC fault isolation considered, $MMC_{1,5}$ are consisted of 60 FBSMs and 70 HBSMs, $MMC_{2,4}$ are consisted of 40 FBSMs and 20 HBSMs, and MMC_3 is consisted of 160 HBSMs. When fault recovery is further considered to ensure continuous power exchange between

the healthy DC grids, 40 and 60 redundant HBSMs need to be added to $MMC_{1,\ 5}$ and $MMC_{2,\ 4}$, respectively. During normal operation, 500MW and 1000MW active power are imported from DC Grid1 and DC Grid2 to DC Grid3, respectively.

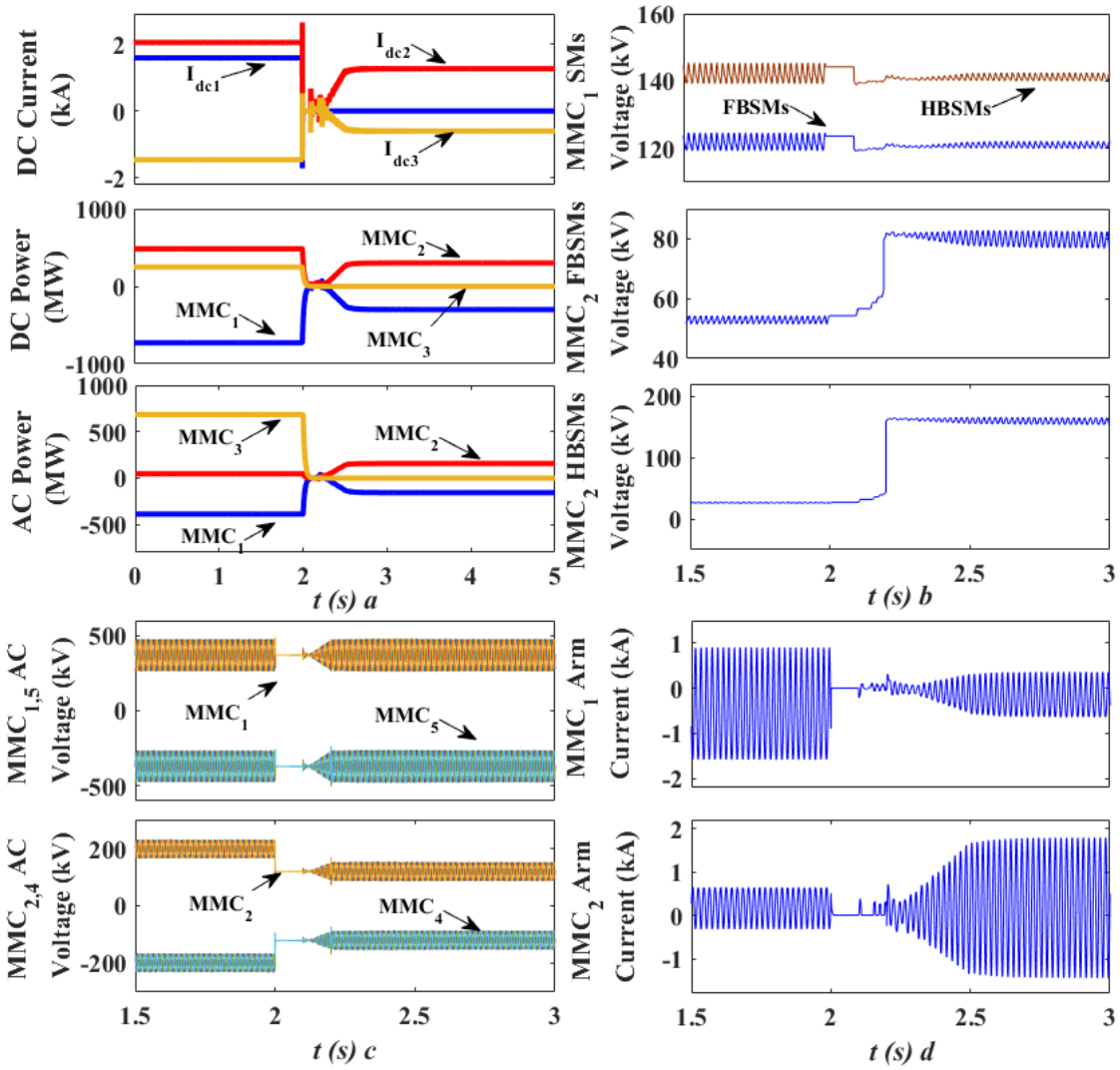


Fig. 6. Simulation results for three-terminal HVDC-AT under low voltage level DC pole-to-pole fault

a DC currents and active power of each converter DC and AC links
b Healthy converter total FBSMs and HBSMs capacitance voltages
c Healthy converter AC voltages
d Healthy converter arm currents

Fig.6 shows the simulation results of the three-terminal HVDC-AT during normal operation, DC fault isolation and continuous operation. As illustrated in Fig. 6, a permanent DC pole-to-pole fault is applied at the MMC_3 DC terminal at 2s. After detecting the DC fault, all the IGBTs in the HVDC-AT are

blocked and the DC currents of each terminal quickly drop to zero. Then the fault line is isolated and the backup line is connected to provide additional current path. After fault isolation, the redundant 60 HBSMs in MMC_2 are activated along with the original 40 FBSMs and 20 HBSMs to avoid over voltage, as shown in Fig. 6b. A ramp signal for the AC voltage reference is provided and the AC-link voltage is built up smoothly to 1 p.u. from 2.1s to 2.2s. $MMC_{2, 4, 5}$ resume power transfer from 2.2s by increasing their active power reference to 156MW within 0.3s, and the maximum active power transfer between DC Grid2 and DC Grid3 after fault recovery decreases from 1000MW to 603MW due to the arm current limit of $MMC_{2, 4}$ (1.82kA). The DC bias voltages of $MMC_{2,4}$ decrease from ±200kV to ±120kV, and the peak arm current of MMC_1 and MMC_2 after fault recovery are 0.69kA and 1.82kA, respectively, which match the previous analysis using (29).

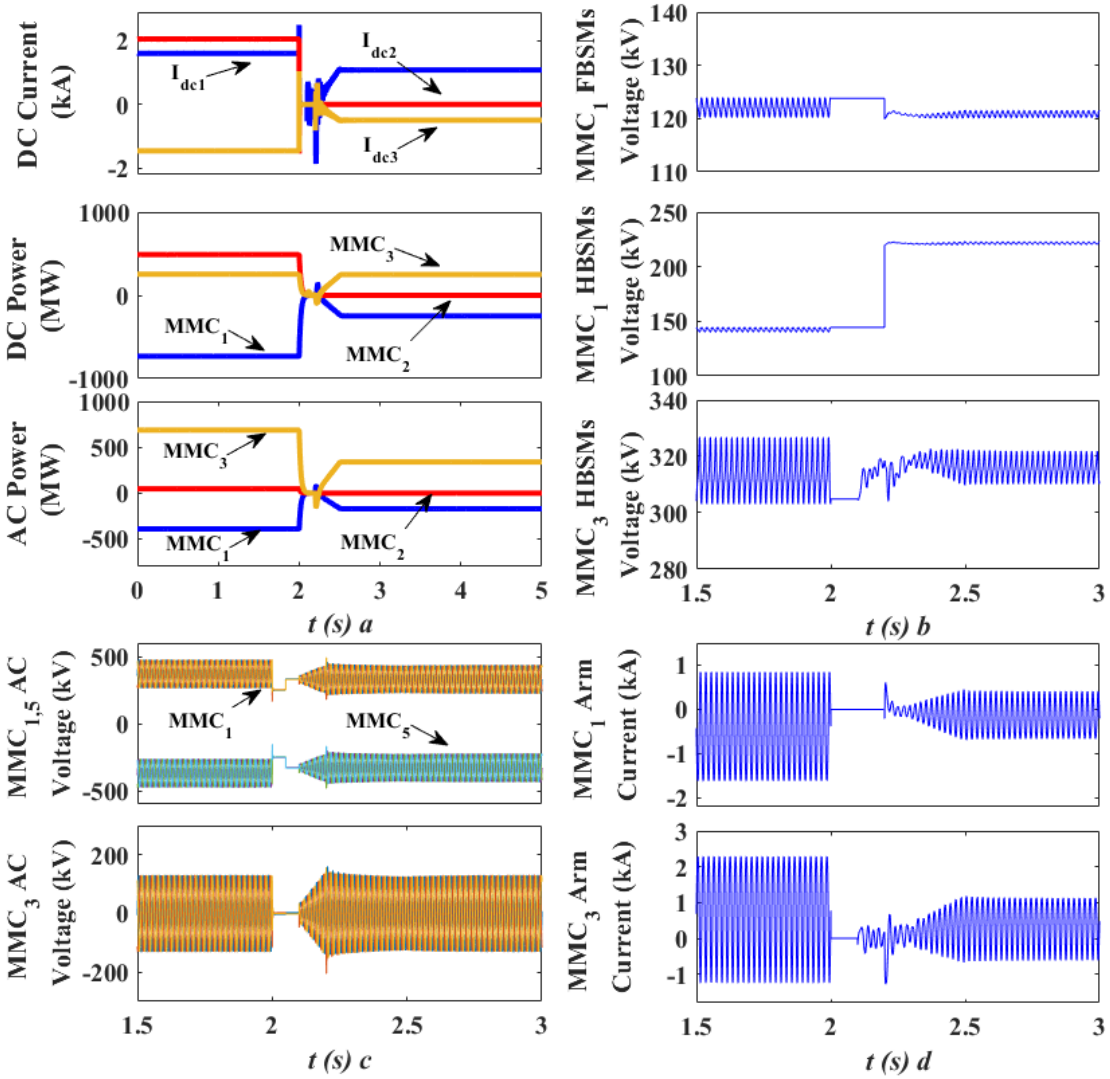


Fig. 7. Simulation results for three-terminal HVDC-AT under medium voltage level DC pole-to-pole fault

a DC currents and active power of each converter DC and AC links
b Healthy converter total FBSMs and HBSMs capacitance voltages
c Healthy converter AC voltages
d Healthy converter arm currents

Fig.7 shows the simulation results for the three-terminal HVDC-AT when a permanent DC pole-to-pole fault is initiated at DC Grid2. After fault isolation, the redundant 40 HBSMs of MMC_1 are activated to avoid over voltage. The DC bias voltages of $MMC_{1,5}$ decrease from ±370kV to ±330kV and the active power transfer between DC Grid1 and DC Grid3 remains at 500MW. The arm currents of MMC_1 and MMC_3 after fault recovery also match well with previous analysis and are all within the range of nominal peak arm current.

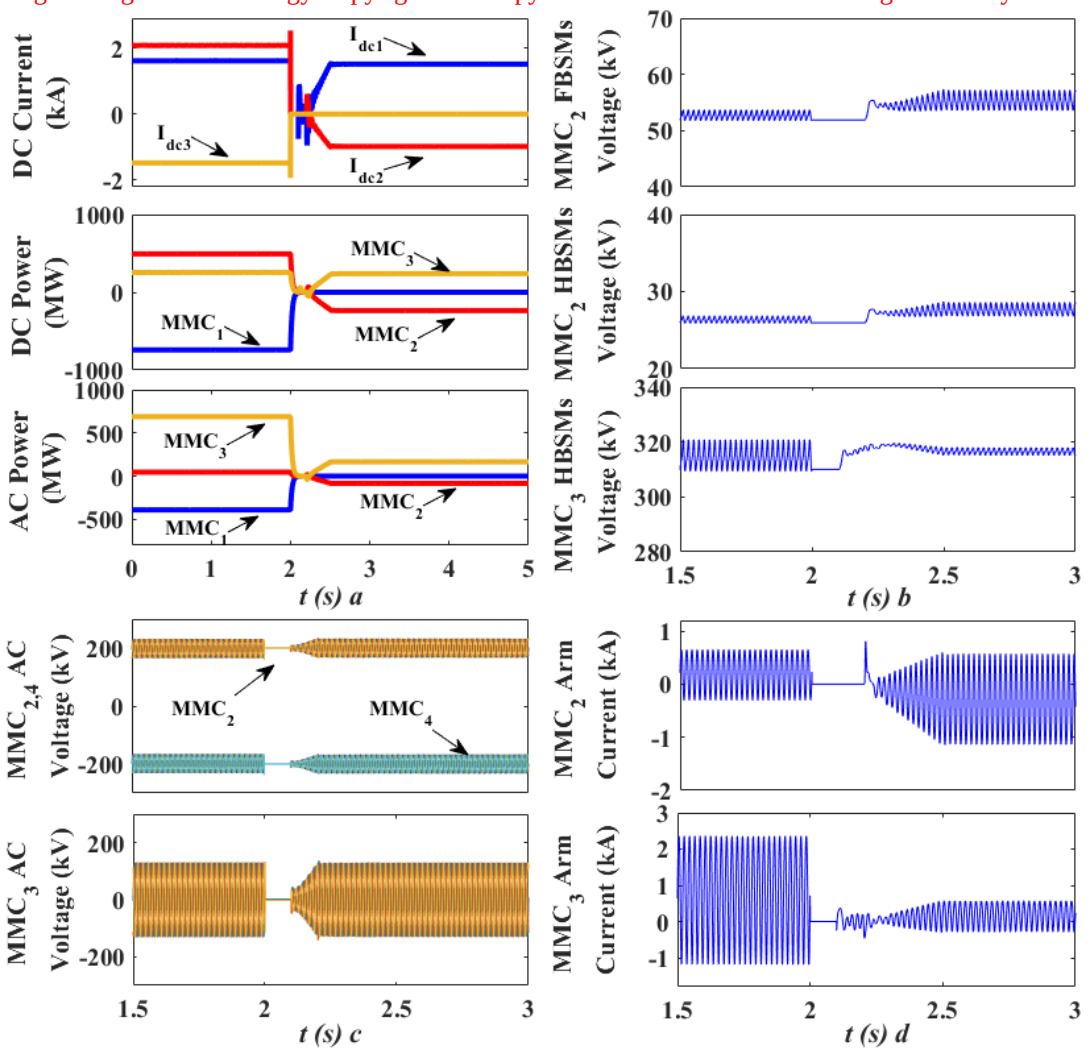


Fig. 8. Simulation results for three-terminal HVDC-AT under high voltage level DC pole-to-pole fault

a DC currents and active power of each converter DC and AC links
b Healthy converter total FBSMs and HBSMs capacitance voltages
c Healthy converter AC voltages
d Healthy converter arm currents

Fig.8 shows the simulation results for the three-terminal HVDC-AT when a permanent DC pole-to-pole fault is applied at DC Grid3. After fault isolation, the AC link voltage control can be switched to healthy converters, e.g. MMC_2, and the active power transfer between DC Grid1 and DC Grid2 can still remain unchanged (500MW).

6. Conclusions

Considering arm current difference, the total number of equivalent semiconductors for the two-terminal and multi-terminal HVDC-ATs with DC fault blocking capability has been studied and compared

with the F2F configuration in this paper. The results show that two-terminal HVDC-AT allows for significant semiconductor savings compared to the F2F for any DC voltage ratio. For multi-terminal systems, the required semiconductors for the two configurations depend on their power ratings and the voltage ratios of the connecting DC grids. Meanwhile, based on the SM configuration analysis, a full operation process for the multi-terminal HVDC-AT considering DC fault has been presented, including normal operation, fault isolation and continuous operation of the healthy converters after fault. The active power exchange among the healthy DC grids may have to be reduced due to the converter arm current limit. Simulation results validate the analysis and demonstrate the effectiveness of the presented SM configuration and the fault recovery scheme of the multi-terminal HVDC-AT.

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