

# Energy Transfer Analysis for Capacitor Voltage Balancing of Modular Multilevel Converters

Binbin Li<sup>1,2</sup>, Rui Li<sup>1</sup>, Barry W. Williams<sup>1</sup>, and Dianguo Xu<sup>2</sup>  
<sup>1</sup>University of Strathclyde, UK, <sup>2</sup>Harbin Institute of Technology, China  
 E-mail: libinbinhit@126.com

**Abstract-** Voltage balancing between sub-module (SM) capacitors is essential for reliable operation of the modular multilevel converter (MMC). To facilitate design and understanding of the balancing controllers, this study presents an energy transfer analysis for MMC, which explains how the energy can be independently transmitted from/to one phase, between the upper and lower arms, and among the SMs, of an MMC. Using this analysis, the variables which can be utilized to achieve capacitor voltage balancing are identified. Validity of this study has been verified by experimental results based on a three-phase MMC prototype.

## I. INTRODUCTION

The modular multilevel converter (MMC) has been regarded as the most promising power converter topology particularly in the field of high-voltage and medium-voltage applications [1]–[2]. The circuit configuration of a three-phase MMC is shown in Fig. 1. Each phase of it consists of two arms, the upper and the lower, which are connected through buffer inductors. Each arm is formed by a series connection of  $N$  nominally identical half-bridge submodules (SMs). Thanks to its modular structure, MMC can be easily expanded to high voltages with nearly ideal sinusoidal shaped output waveforms and a very high efficiency. However, MMC benefits but also suffers from the series connection of half-bridge SMs. One specific issue associated with MMC is that the voltage unbalance may occur among the capacitors of different SMs. Capacitor voltage balancing strategies must be employed to mitigate the voltage unbalance [2]–[6]. However, so far, although there are many kinds of voltage balancing strategies, the basic principle to realize this voltage balancing is not clear. Most of these methods have not clearly shown what variables can be controlled and why it works. Therefore,

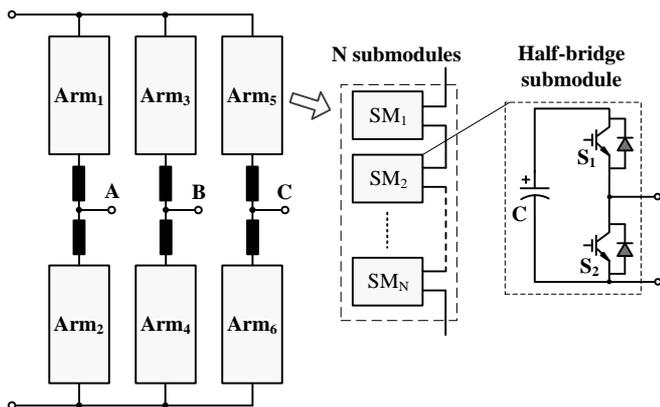


Fig. 1 Circuit configuration of the modular multilevel converter (MMC)

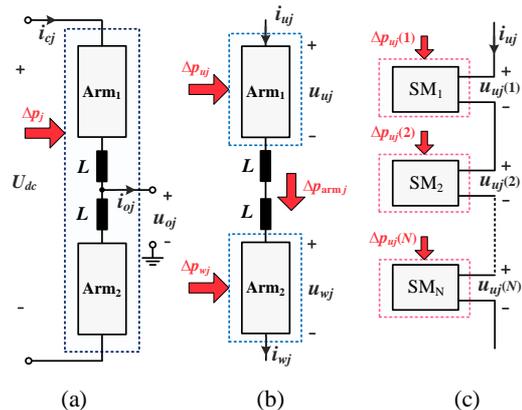


Fig. 2: Energy transfer analysis in an MMC, (a) phase energy transfer analysis, (b) Arm energy transfer analysis, (c) SM energy transfer analysis.

this paper aims give a mathematical analysis of the energy transfers within MMC, which reveals how the voltage balancing can be achieved by appropriately redistribute the energy. This study helps understanding and design of the voltage balancing controllers. Finally, validity of this analysis has been verified experimentally on a three-phase MMC prototype.

## II. ENERGY TRANSFER ANALYSIS OF MMC

Regarding a balanced three-phase MMC system, the stored energy should be uniformly distributed among the three phases, between the upper and the lower arms of each phase, and among all the SMs within each arm. Thus ideally, the dc-bus voltage  $U_{dc}$  should be equally shared among the SM capacitors in the same arm, that is

$$U_{cap\_uj,0}(i) = U_{cap\_wj,0}(i) = U_{dc}/N \quad (1)$$

where  $U_{cap\_uj,0}(i)$  and  $U_{cap\_wj,0}(i)$  are the dc value of the capacitor voltages of the  $i$ -th SM in the upper and the lower arm of phase  $j$ , respectively.

However, in practice, MMC cannot be naturally balanced due to component parametric differences or inconsistent control signal delays. Thus the capacitor voltage unbalance will inevitably occur. The way to restrain the uneven energy distribution is by redistributing the energy. Therefore, in this section, a top-down analysis is presented to investigate how the energy can be transferred inside an MMC from the perspective of three layers: phase, arm, and SM. In addition, the constraints are also deduced to reveal that how the energy transfer of the lower layer will not influence the energy stored in the upper layers.

### A. Phase Energy Transfer

As shown in Fig. 2(a), the absorbed instantaneous power of one phase of MMC is given by

$$\Delta p_j = U_{dc} i_{cj} - u_{oj} i_{oj} \quad (2)$$

The ac-side voltage  $u_{oj}$  and current  $i_{oj}$  can be expressed as

$$u_{oj} = \hat{u}_{oj} \cos(\omega_1 t) \quad (3a)$$

$$i_{oj} = \hat{i}_{oj} \cos(\omega_1 t - \varphi) \quad (3b)$$

where  $\hat{u}_{oj}$  and  $\hat{i}_{oj}$  are the amplitudes,  $\omega_1$  is the angular frequency of the output voltage, and  $\varphi$  is the power factor angle. In steady-state conditions, the average absorbed power of this phase can be obtained as

$$\Delta P_j = U_{dc} I_{cj,0} - \frac{1}{2} \hat{u}_{oj} \hat{i}_{oj} \cos(\varphi) \quad (4)$$

where  $I_{cj,0}$  is the dc component of the circulating current  $i_{cj}$ . Defining the total power loss of phase  $j$  as  $P_{loss\_j}$ , then the following equation must be satisfied in order to maintain the energy balance of this phase  $\Delta P_j = P_{loss\_j}$ .

According to (4), there are five ways to vary the absorbed power of phase  $j$ , including the regulation of  $U_{dc}$ ,  $\hat{u}_{oj}$ ,  $\hat{i}_{oj}$ ,  $\varphi$ , and  $I_{cj,0}$ . However, as the first four quantities are fixed (when MMC operates as an inverter,  $U_{dc}$  is always immutable while  $\hat{u}_{oj}$ ,  $\hat{i}_{oj}$ , and  $\varphi$  are maintained stable by the overall control command of active/reactive power; on the other hand, when MMC acts as a rectifier,  $\hat{u}_{oj}$  is the grid voltage while  $U_{dc}$ ,  $\hat{i}_{oj}$ , and  $\varphi$  are kept stable by the overall control), the only controllable quantity is the dc component of the circulating current  $I_{cj,0}$ . And  $I_{cj,0}$  can be controlled by adjusting the dc component of the common mode arm voltage, i.e.,  $U_{comj,0}$ .

### B. Energy Transfer Between Arms

After accomplishing the phase balance, the next step is to ensure that energy of the upper and the lower arms are balanced, respectively, that is

$$\Delta P_{uj} = P_{loss\_uj} \quad (5a)$$

$$\Delta P_{wj} = P_{loss\_wj} \quad (5b)$$

where  $\Delta P_{uj}$  and  $\Delta P_{wj}$  are respectively, the average absorbed power of the upper arm and the lower arm, whose summation is  $\Delta P_j$ .  $P_{loss\_uj}$  and  $P_{loss\_wj}$  are the power losses of the upper and lower arms, respectively, and whose summation is  $P_{loss\_j}$ . Hence, to not disturb the phase energy balance, it is concluded that the arm balance can only be achieved by forming an energy exchange between the upper and lower arms, which gives the constraint of  $\Delta P_{uj} + \Delta P_{wj} = \Delta P_j$ .

As shown in Fig. 2(b), the absorbed instantaneous power of each arm can be given by

$$\Delta p_{uj} = u_{uj} i_{uj} \quad (6a)$$

$$\Delta p_{wj} = u_{wj} i_{wj} \quad (6b)$$

By defining common mode voltage  $u_{comj} = 0.5(u_{uj} + u_{wj})$  and differential mode voltage  $u_{diffj} = 0.5(u_{uj} - u_{wj})$ , we have

$$\Delta p_{uj} = (u_{comj} - u_{diffj}) \left( i_{cj} + \frac{1}{2} i_{oj} \right) \quad (7a)$$

$$\Delta p_{wj} = (u_{comj} + u_{diffj}) \left( i_{cj} - \frac{1}{2} i_{oj} \right). \quad (7b)$$

Then, the instantaneous power transferred from the upper arm to the lower arm can be derived as

$$\Delta p_{armj} = \frac{1}{2} (\Delta p_{wj} - \Delta p_{uj}) = u_{diffj} i_{cj} - \frac{1}{2} u_{comj} i_{oj}. \quad (8)$$

However, when MMC operates under normal conditions, the average value of (8) is always zero ( $\Delta P_{armj} = 0$ ) since  $u_{comj}$  and  $i_{cj}$  are both dc quantities (i.e.,  $u_{comj} = U_{comj,0}$ ,  $i_{cj} = I_{cj,0}$ ) whereas  $i_{oj}$  and  $u_{diffj}$  are both ac quantities. Note that  $u_{diffj}$  can be expressed as

$$u_{diffj} = \hat{u}_{diffj} \cos(\omega_1 t + \delta) \quad (9)$$

where  $\hat{u}_{diffj}$  is amplitude,  $\delta$  is the phase angle between  $u_{oj}$  and  $u_{diffj}$ . According to (8), if a nonzero power transfer  $\Delta P_{armj}$  is required, components at other frequencies must be introduced and there are three possible approaches:

- 1) introducing a dc offset onto the differential mode arm voltage  $u_{diffj}$  or the output current  $i_{oj}$ ;
- 2) injecting a zero-sequence component into  $u_{diffj}$  as well as the circulating current  $i_{cj}$  [6];
- 3) adding a fundamental ac component in the common mode voltage  $u_{comj}$ , generating an ac component in  $i_{cj}$ .

Note that the first approach is infeasible since no dc offset is allowed to appear at the output of inverters. The latter two approaches are both available; however, the third approach is preferred as it can generate a less amplitude of the circulating current than the second approach (since amplitude of the injected zero-sequence voltage in the second approach is small, to transfer the same amount of power, current amplitude has to be higher).

Therefore, by adding a fundamental frequency component ( $u_{comj,1}$  and  $i_{cj,1}$ ) to  $u_{comj}$  and  $i_{cj}$ , the transferred power between the arms can be rewritten as

$$\Delta p_{armj} = \hat{u}_{diffj} \cos(\omega_1 t + \delta) \times (I_{cj,0} + \hat{i}_{cj,1} \cos(\omega_1 t + \phi)) - (U_{comj,0} + \hat{u}_{comj,1} \cos(\omega_1 t + \phi + 90^\circ)) \times \frac{\hat{i}_{oj}}{2} \cos(\omega_1 t - \varphi) \quad (10)$$

where  $\hat{i}_{cj,1}$  and  $\phi$  are the amplitude and phase angle of  $i_{cj,1}$ ,  $\hat{u}_{comj,1}$  is the amplitude of  $u_{comj,1}$  and is given by

$$\hat{u}_{comj,1} = \omega_1 L \hat{i}_{cj,1} \quad (11)$$

Then, the average value of (10) can be obtained as

$$\Delta P_{armj} = \frac{1}{2} \hat{u}_{diffj} \hat{i}_{cj,1} \cos(\delta - \phi) - \frac{1}{4} \omega_1 L \hat{i}_{oj} \hat{i}_{cj,1} \cos(\phi + \varphi + 90^\circ) \quad (12)$$

Since MMC is always used in high voltage applications, the following relationship exists:

$$\frac{1}{2} \omega_1 L \hat{i}_{oj} \ll \hat{u}_{diffj}. \quad (13)$$

Hence, Eq. (12) can be approximated as

$$\Delta P_{armj} = \frac{1}{2} \hat{u}_{diffj} \hat{i}_{cj,1} \cos(\delta - \phi). \quad (14)$$

If  $\Delta P_{armj} > 0$ , it means that the lower arm is charging while the upper arm is discharging, and vice versa. It is also seen that the minimum peak value of the circulating current can be found when the phase angle of  $i_{cj,1}$  is selected as  $\phi = \delta$ , which means  $i_{cj,1}$  should be in phase with  $u_{diffj}$ . Furthermore, as only

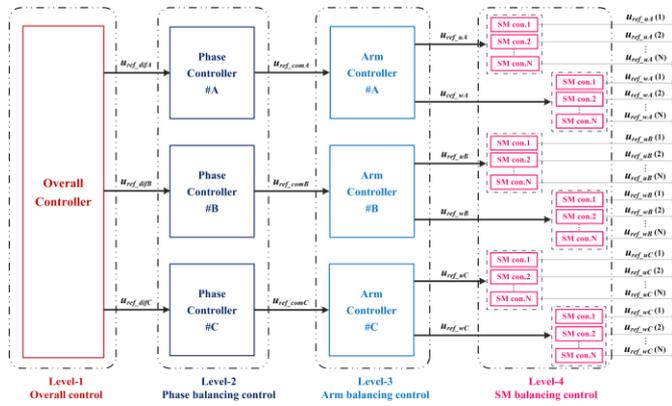


Fig. 3 Proposed hierarchical voltage balancing control scheme.

an ac component circulating current ( $i_{cj,1}$ ) is employed in the process of arm energy transfer, according to (4), it will not conflict with the behavior of the previously mentioned phase energy transfer.

### C. Energy Transfer Among SMs

As discussed, the stored energy in each phase and each arm can be controlled independently. Further, this section will take into account the energy transfer of every particular SM.

According to Fig. 2(c), for an upper-arm SM, the absorbed instantaneous power can be obtained as follows:

$$\Delta p_{ij}(i) = u_{ij}(i)i_{ij} = \left( \frac{u_{ij}}{N} + \Delta u_{ij}(i) \right) \left( i_{cj} + \frac{1}{2}i_{oj} \right) \quad (15)$$

where  $\Delta u_{ij}(i)$  is the output voltage adjustment of the  $i$ -th SM in the upper arm. Since the arm current  $i_{ij}$  is immutable (it is determined by the higher level controllers), the only controllable parameter is  $\Delta u_{ij}(i)$ . Note that whether a dc component or a fundamental frequency component of  $\Delta u_{ij}(i)$  is able to form an active power transfer into the SM. Meanwhile, to not influence the processes of the arm energy transfer and the phase energy transfer, the sum of  $\Delta p_{ij}(i)$  in the upper arm must be kept constant. This gives the following constraint for  $\Delta u_{ij}(i)$ :

$$\sum_{i=0}^N \Delta u_{ij}(i) = 0. \quad (16)$$

## III. VOLTAGE BALANCING CONTROL SCHEME

Based on previous energy transfer analysis of MMC, in this section, the voltage balancing control is implemented, consisting of an overall control, a phase balancing control, an arm balancing control, and a SM balancing control, as shown in Fig. 3. These control layers are organized in a top-down structure, in which the balancing control of MMC is refined gradually from the overall system to each phase, then to each arm, and finally to each SM. In contrast to the balancing control method in [5], several improvements are proposed to enhance the control stability and tracking accuracy. Most importantly, these control layers are totally decoupled from each other, in other words, the lower layer controller will not conflict with the performances of the upper layer controllers.

### A. Level 1 - Overall Control

The primary control level is the overall control, which takes control of MMC as a conventional three-phase voltage source converter (VSC). Fig. 4 presents the control block diagram of the overall controller. It comprises the dc-bus voltage (or the active power) regulation and the reactive power regulation. Moreover, the classical PI regulators as well as the  $d-q$  decoupling current control scheme are adopted. The outputs of the overall control loop are the reference signals for the differential mode arm voltage of MMC, i.e.,  $u_{ref\_diff}$ .

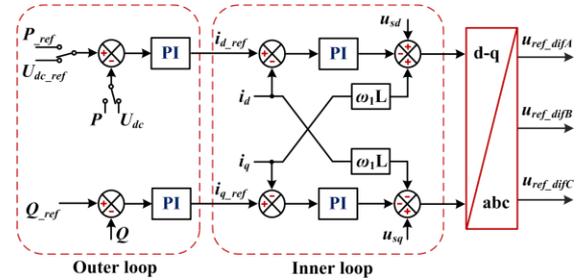


Fig. 4. Block diagram of the overall controller.

### B. Level 2 - Phase Balancing Control

The secondary control level (phase balancing control) ensures that the energy stored in one phase of MMC is maintained balanced by adjusting the dc component of the circulating current. As depicted in Fig. 5(a), the dc-bus voltage  $U_{dc}$ , is used as the command and compared with one half of the sum of the SM capacitor voltages in phase  $j$ , that is

$$u_{sum\_cap\_j} = \frac{1}{2} \sum_{i=1}^N (u_{cap\_uj}(i) + u_{cap\_wj}(i)). \quad (17)$$

Then, a PI controller is adopted to mitigate this voltage difference and generate the reference of the dc circulating current  $I_{cj,0}^*$ , where  $K_{p1}$  and  $K_{i1}$  are the control parameters, and  $U_{sum\_cap\_j,0}$  denotes the dc value of  $u_{sum\_cap\_j}$ . Note that since the PI controller is sensitive to the harmonics in the capacitor voltages, a moving average filter (MAF) is added to obtain the dc value of  $u_{sum\_cap\_j}$ .

### C. Level 3 - Arm Balancing Control

The control block diagram of the arm balancing control is shown in Fig. 5(b), in which the summation of the lower-arm capacitor voltages and that of the upper-arm capacitor voltages are kept equal by regulating the fundamental frequency component of the circulating current, as discussed in previous section.  $K_{p2}$  and  $K_{i2}$  are the PI control parameters,  $U_{sum\_cap\_wj,0}$  and  $U_{sum\_cap\_uj,0}$  respectively represent the dc value of the summation of the lower-arm and upper-arm SM capacitor voltages:

$$u_{sum\_cap\_wj} = \sum_{i=1}^N u_{cap\_wj}(i) \quad (18a)$$

$$u_{sum\_cap\_uj} = \sum_{i=1}^N u_{cap\_uj}(i) \quad (18b)$$

Similarly,  $U_{sum\_cap\_wj,0}$  and  $U_{sum\_cap\_uj,0}$  are obtained by adding a MAF in the path.

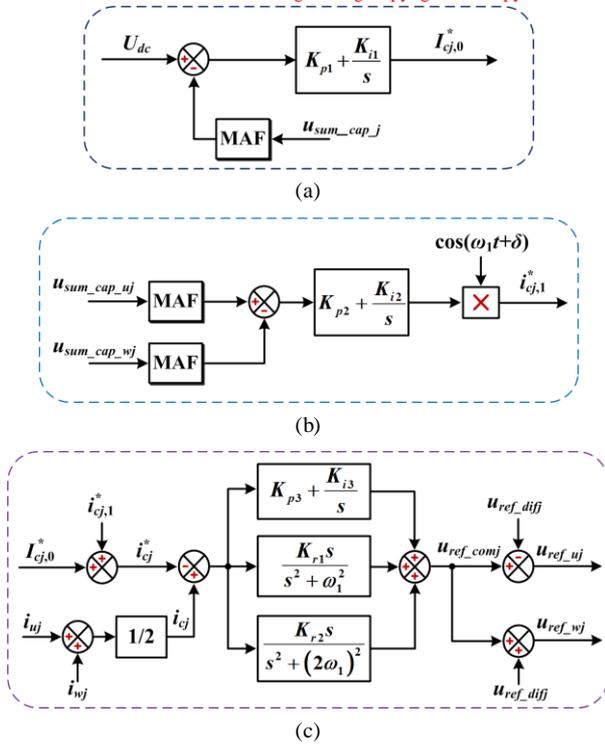


Fig. 5. Block diagram of the phase balancing controller and the arm balancing controller: (a) Phase balancing controller. (b) Arm balancing controller. (c) Inner circulating current controller.

Furthermore, an inner current control loop is built, as shown in Fig. 5(c), which forces the circulating current to follow the reference. As there are mainly three dominated frequency components in the circulating current: the dc component for phase balancing, the fundamental frequency component for arm balancing, and the second order component which should be suppressed, the conventional PI controller adopted exhibits two well-known drawbacks: the inability of tracking these sinusoidal references without steady-state error and a poor disturbance rejection capability. Therefore, in this paper, the proportional-integral-resonant (PIR) controller comprising two resonant terms has been employed due to its sufficiently high gain at selected frequencies, that is

$$G_{PIR}(s) = K_{p3} + \frac{K_{i3}}{s} + \frac{K_{r1}s}{s^2 + \omega_1^2} + \frac{K_{r2}s}{s^2 + (2\omega_1)^2} \quad (19)$$

where  $K_{p3}$ ,  $K_{i3}$ ,  $K_{r1}$ , and  $K_{r2}$  refer to the control parameters of the PIR controller, and the resonant frequencies are tuned to the fundamental and second order frequencies, respectively.

Thus, the references for the upper-arm voltage as well as the lower-arm voltage can be obtained, respectively

$$u_{ref\_uj} = u_{ref\_comj} - u_{ref\_diff} \quad (20a)$$

$$u_{ref\_wj} = u_{ref\_comj} + u_{ref\_diff} \quad (20b)$$

#### D. Level 4 - SM Balancing Control

Finally, Fig. 6(a) shows the control block diagram of the SM balancing control. Different from the conventional individual-balancing method shown in [5], here the instantaneous average voltage of the capacitors in one arm

has been selected as the control command so as to decouple it from the upper layer controllers.

Taking an upper-arm SM as an example:

$$u_{ref\_uj}(i) = \frac{u_{ref\_uj}}{N} + K_{p4} \left( \frac{u_{sum\_cap\_uj}}{N} - u_{cap\_uj}(i) \right) \times \text{sign}(i_{uj}) \quad (21)$$

where  $K_{p4}$  denotes the proportional gain, “ $\text{sign}(x)$ ” represents the signum function (i.e.,  $\text{sign}(x)=1$  when  $x \geq 0$ , whereas  $\text{sign}(x)=-1$  when  $x < 0$ ). The generated reference  $u_{ref\_uj}(i)$  will be eventually introduced to the corresponding PWM modulator to generate final gating signals.

The sum of  $u_{ref\_uj}(i)$  in the upper arm can be calculated as

$$\sum_{i=1}^N u_{ref\_uj}(i) = u_{ref\_uj} + K_{p4} \left( u_{sum\_cap\_uj} - \sum_{i=1}^N u_{cap\_uj}(i) \right) \times \text{sign}(i_{uj}) \quad (22)$$

Substituting (18a) into (22) yields

$$\sum_{i=1}^N u_{ref\_uj}(i) = u_{ref\_uj} \quad (23)$$

which is equivalent to (16), meaning that the proposed SM balancing control will not affect the performances of the upper layer controllers.

Similarly, for the lower-arm SMs, the same conclusion can be drawn and the control loop is shown in Fig. 6(b).

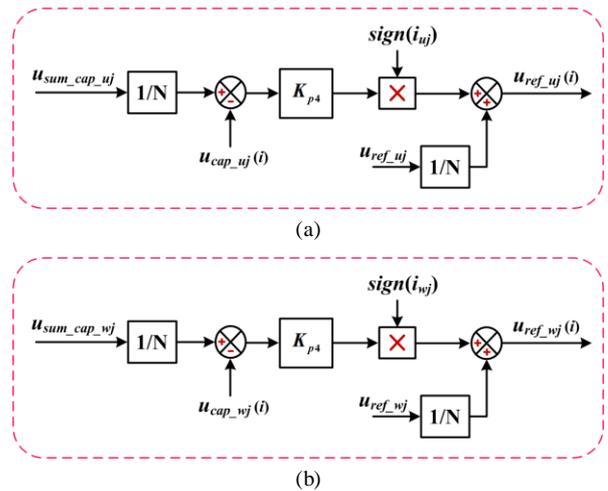


Fig. 6. Block diagram of the SM balancing controller. (a) Upper-arm SM controller. (b) Lower-arm SM controller.

## IV. EXPERIMENTAL VERIFICATION

### A. System Configuration

In order to verify the validity of the energy transfer analysis and the voltage balancing method, a three-phase MMC prototype with three SMs per arm has been built, as shown in Fig. 7. The circuit parameters and operating conditions are listed in Table I. The dc-bus voltage is obtained by using a three-phase diode rectifier, and the command of the overall controller is set as  $P=1.6\text{kW}$  and  $Q=0\text{Var}$ .

As for the controller, a TMS320F28335 DSP is used to generate the three-phase sinusoidal references while an EP3C25Q240C8 FPGA is adopted to generate the triangular carriers with appropriate phase-shift angle and send the PWM

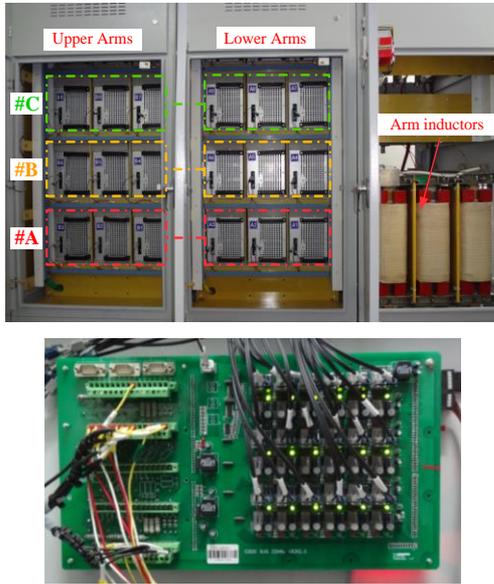


Fig. 7: MMC Prototype and the control board.

signals to SMs via optical fibers. Each SM is controlled by an EPM570T100 CPLD, which receives the PWM signals and sends back the monitored capacitor voltage.

Furthermore, a significant power loss unbalance is created intentionally, where a  $1k\Omega$  resistor is shunted to the capacitor of SM<sub>3</sub> in the lower arm of phase A. Thus, in steady states,

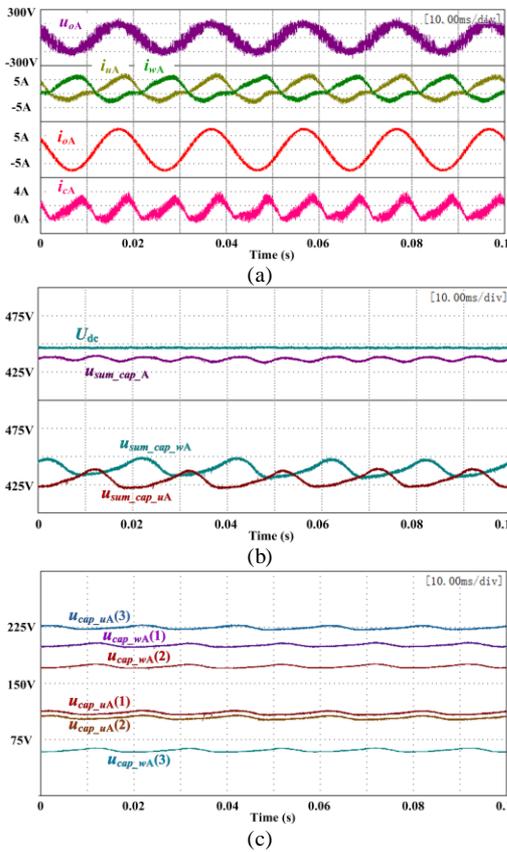


Fig. 8: Experimental waveforms without balancing control.

there would be a maximum of 22.5W shunt loss difference among the SMs, between the lower and upper arms, and among the three phases.

Table 1 Laboratory prototype specifications

Quantity	Value
Number of SMs per arm	$N=3$
DC-bus voltage	$U_{dc}=450V$
Rated active power	$P=2kW$
Rated reactive power	$Q=0Var$
Fundamental frequency	$f_o=50Hz$
Rated SM capacitor voltage	$U_{cap}=U_{dc}/3=150V$
SM capacitance	$C_{sm}=1867\mu F$
Buffer inductors	$L_u=L_w=5mH$
Carrier frequency	$f_c=4kHz$
Load resistance	$20\Omega$

### B. Experimental Results

Fig. 8 presents the experimental results without any balancing control method. It is clear that there is a severe disparity among the SM capacitor voltages with a maximum difference of 125V and the highest capacitor voltage (SM3 in the upper arm) goes up to 225V, which is much higher than the rated capacitor voltage. Meanwhile, as can be observed,  $u_{sum\_cap\_A}$  is about 9V lower than  $U_{dc}$ , and  $u_{sum\_cap\_uA}$  is 10V higher than  $u_{sum\_cap\_wA}$ . It also can be seen that the arm currents  $i_{uA}$  and  $i_{wA}$  are clearly distorted because of the existence of the second-order(100Hz) harmonics in  $i_{cA}$ .

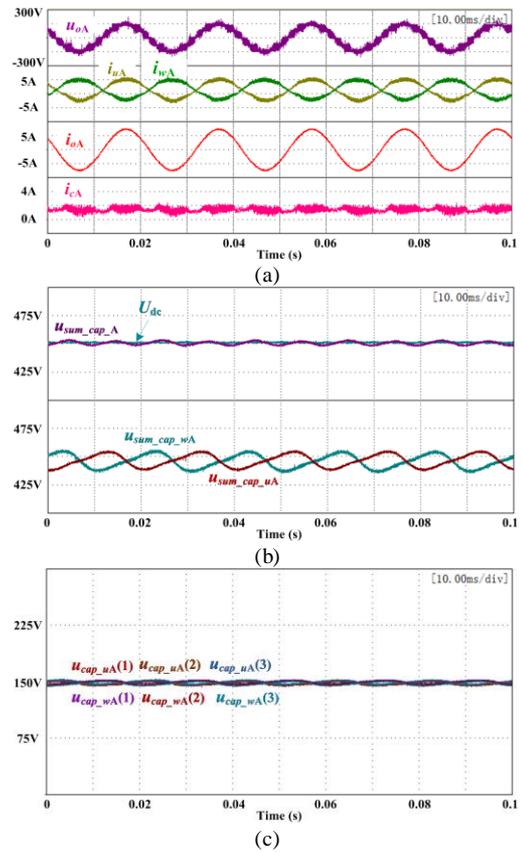


Fig. 9: Experimental waveforms with balancing control.

Fig. 9 shows the experimental results with the proposed hierarchical balancing control scheme. Compared to Fig. 8, we can see that all the SM capacitor voltages are kept constant with the value of 150V and in the meantime,  $u_{sum\_cap\_A}$  is regulated equal to  $U_{dc}$  and  $u_{sum\_cap\_uA}$  is also equal to  $u_{sum\_cap\_wA}$ . This means that the energy stored in MMC is evenly distributed among the phases, between the upper and the lower arms, and among all the SMs, which confirms the effectiveness of the hierarchical balancing controllers. Besides, the peak values and distortions of  $i_{uA}$  and  $i_{wA}$  are both reduced, because the second-order harmonics of the circulating current  $i_{cA}$  is basically eliminated by the inner PIR current control loop.

Besides, further experiments are performed to test the stability of the proposed balancing control scheme by intentionally imposing some disturbances. Fig. 10 shows the experimental waveforms with the response to a ramp change of the dc-bus voltage (with a slope of 0.45V/ms). As can be seen, the balancing controllers are stable during this transient and, in the meantime, the capacitor voltages are kept well balanced without any significant deviations. Note that although  $u_{sum\_cap\_A}$  may be temporarily higher than  $U_{dc}$  after the transient change, which means an overshoot, it reaches its new steady-state value quickly.

## V. CONCLUSION

In this paper, an energy transfer analysis has been given for the operation of MMC. It explained how the capacitor voltage balancing can be achieved within the phase, between the arms, and among the SMs. Based on this analysis, the variables which can be utilized to perform voltage balancing are identified. The voltage balancing controllers are then proposed for the operation of MMC, in which the balancing task is refined gradually from the higher control layers to the lower control layers. Moreover, these control layers are decoupled from each other thus the control parameters are easy to design and the whole control system has strong stability and robustness. Finally, a three-phase MMC prototype was tested in the laboratory. Experimental results confirm the validity of the proposed hierarchical balancing control method and show very good static and dynamic performances.

## VI. ACKNOWLEDGEMENT

This research was supported by EPSRC grant EP/K006428/1 <http://gow.epsrc.ac.uk/NGBOViewGrant.aspx?GrantRef=EP/K006428/1>

## REFERENCES

- [1] [1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE PowerTech. Conf.*, Bologna, Italy, Jun. 23–26, 2003, vol. 3.
- [2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [3] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.
- [4] A. Dekka, B. Wu, and N. R. Zargari, "A novel modulation scheme and voltage balancing algorithm for modular multilevel converter," *IEEE Trans. Ind. App.*, vol. 52, no. 1, pp. 432–443, Jan. 2016.
- [5] M. Hagiwara and H. Akagi, "Control and analysis of the modular multilevel cascade converter based on double-star chopper-cells (MMCC-DSCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1649–1658, Jun. 2011.
- [6] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation-suppression method of floating capacitors in a new modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1943–1954, May 2013.

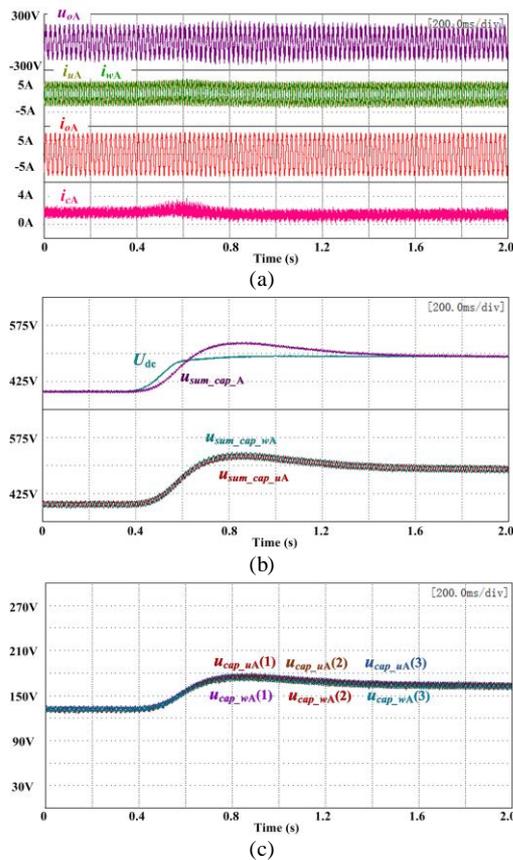


Fig. 10: Dynamic response with a ramp change of the dc-bus voltage