# Operation and Control Design of New Three-phase and Single-phase DC/AC inverters with Reduced Number of Switches

*Abstract*—**Inverters with reduced number of switches have been proposed in the literature to improve the capability of cost reduction, total inverters size and switching losses of dc/ac inverter topologies. In addition, they have a lower probability of damaging the semi-conductor switches as well as lower common-mode currents. This paper proposes new designs for inverters with reduced number of switches. For three-phase systems, the proposed inverters use four switches instead of six in the traditional three-phase Voltage Source Inverter (VSI). Compared to the traditional Four-switch three-phase (FSTP) inverter, the proposed FSTP inverters improve the voltage utilization factor of the input dc supply. Classical controllers as well as sliding mode controller are used to discuss the dynamic response and robustness of the inverters. In addition, the paper presents new single-phase inverters with two switches instead of four in the traditional VSI. The capability of suppressing the 2nd order current harmonic from the input dc side is discussed. Equations explaining the control design, switches ratings, and the operation of the proposed inverters are presented in this paper. The basic structure, control design, and MATLAB/SIMULINK results are presented. Practical results substantiate the design flexibility of the proposed topologies when controlled by a TMSF280335 DSP.**

***Keywords-component; dc/ac inverters; sliding mode controllers; PR controllers; Four-switch three-phase inverter (FSTP)***

## I. INTRODUCTION

The governmental agencies insistence to reduce the CO2 generation created an international interest in power system and micro-grid research and development [1]. Recently, numerous inverter topologies are presented to improve the operation of micro-grid systems.

For a long period, the conventional six-switch three-phase (SSTP) two-level voltage source inverter (VSI) has been the most common converter topology for many applications such as renewable energy conversion systems, motor drives, and wind turbine systems. However, converter topologies with reduced switches number are demanded in some low power applications, such as photovoltaic, fuel cells and electric vehicles, in order to reduce the cost, size and increase the system's efficiency. A novel three-phase two-level VSI with only four switches was implemented in [2], see Fig.1. In this Four-switch three-phase (FSTP) inverter, two of the output load voltages are fed from the two legs of the inverters while the third phase is fed directly from the dc side.

In comparison with the conventional VSI, the FSTP inverter has important features such as lower cost, higher efficiency, reduced number of measurement boards, gate drives and the real-time calculations [3]. In addition, the FSTP inverter reduces the maximum common mode voltage by 33% in comparison with the SSTP inverter [3, 4]. Because of the reduced interaction between the switches, the FSTP inverter decreases the probabilities of damaging the switches. The main disadvantage of the FSTP is that the maximum output voltage could be obtained across the load is limited to 28.28% of the input dc voltage [2]. Another disadvantage of the conventional FSTP is that the third phase of output load is fed from the dc side which may generate dc current components in the output three-phase currents. These dc current components are hazardous and a proper control effort should be conducted in order to suppress them. IEEE 1574 standards restrict the dc current components to < 0.5% of the rated RMS current while IEC 61727 standards limit them to <1%. In addition, the fluctuation of the dc-link capacitors at the fundamental frequency results in fluctuations of the output voltages and currents of the FSTP inverter [5]. The problem of dc-link voltage oscillation necessitates a modified pulse-width modulated (PWM) signals to control and create the desired output voltage during the switching period [3]. Practically, the dc-link split capacitors may not have exactly equal capacitance values. Consequently, over-modulation of switch PWM process may occur to keep the dc-link midpoint voltage constant [5]. The operation, control design, and performance of the FSTP have been discussed extensively in the literature [3]-[11]. In [12], a FSTP inverter based on the conventional SEPIC converter is implemented and controlled with sliding mode control. The reachable output voltage of the SEPIC-based FSTP inverter has been shown to be double the voltage of the conventional FSTP inverter at the same conditions. In addition, the inverter solved the problem of the circulating current in the dc-link capacitors. However, like the conventional FSTP, the SEPIC-based inverter is fed from the input dc side directly and hence; dc currents components may be injected into the ac grid.

Out of the thirty three basic dc-dc converters, there are four bidirectional converters capable of providing output voltage with positive and negative polarities. These converters are shown in Fig.2 as two voltage buck and two voltage boost converters. Based on these converters, new three-phase inverters with four switches can be generated. Unlike the other FSTP inverters, the proposed inverters do not have direct connection between the ac phases and the dc side voltage. Consequently, the problem of dc currents injection in the ac grid does not exist. Moreover, because they do not require the direct connection between the ac and dc sides, the proposed converters can operate as dc/ac inverters and ac/dc rectifiers. In dc/ac inversion mode, the proposed inverters double the

maximum output three-phase voltage in compare with the conventional FSTP inverter.

Unfortunately, the proposed converters are time variant systems where the overall transfer function describing the relation between the input and output voltages and currents depends on the switching periods of the switches. This results in a complex stable design because the converter poles and zeros travel through a long trajectory. Moreover, the time-varying transfer function leads to output voltage and current distortion [13, 14]. Converter stability and reliability decreases with increasing passive elements values. However, reducing the inductors and capacitors values results in larger high frequency ripple currents and voltages components and hence, increases the total harmonic distortion (THD) of the output current and voltage. On the other hand, increasing the passive elements values increases the stored energy inside the inverter producing third order harmonic component and its multiples in the input dc current.

This paper presents new inverter/rectifier topologies with reduced switches number based on the abovementioned bidirectional dc-dc converters. Moreover, the paper explains the normal operation and proposes beneficial comparisons and performance evaluation of the proposed inverters. In addition, the proper control design of the proposed converters is presented with sliding mode control techniques (SMC). Practical results substantiate the design flexibility of the proposed topologies when controlled by a TMSF280335 DSP.

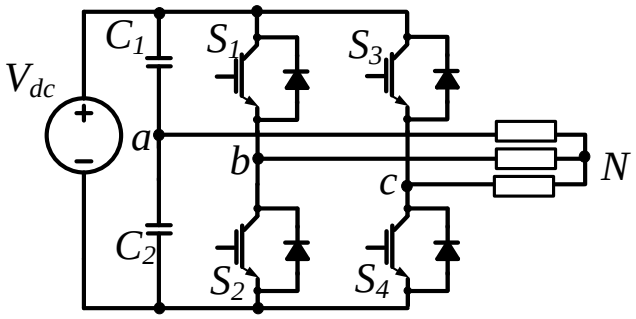



Fig.1. Conventional Four-switch three-phase inverter (FSTP)

## II. DC-DC Converters with Positive and Negative Output Voltage

The four two-switch two-diode dc-dc converters with positive and negative output voltages are shown in Fig.2. Two of these converters are voltage buck converters (b1G and b2G) while the other two are voltage boost converters (B1G and B2G). The relation between output voltage ($V_o$) and the input voltage ($V_{in}$) is defined by voltage conversion ratio (M) as:

$$M(D) = V_o / V_{in} \quad (1)$$

Where D is the converter duty ratio and can be defined as:

$$D = t_{on} / t_s \quad (2)$$

Where $t_{on}$ is the duration when switch $S_1$ is on while $t_s$ is the total switching period.

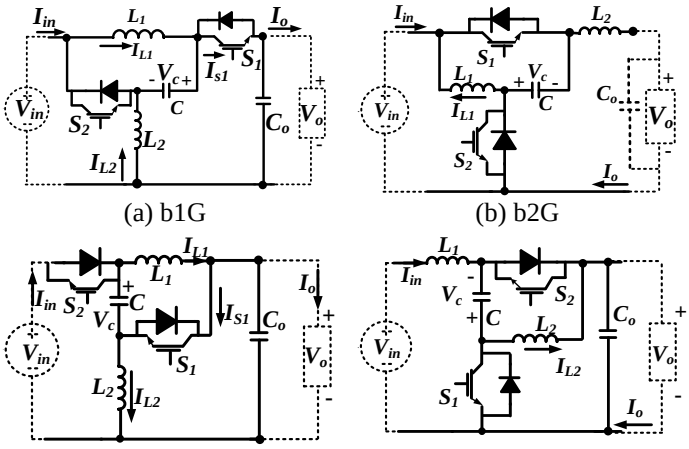


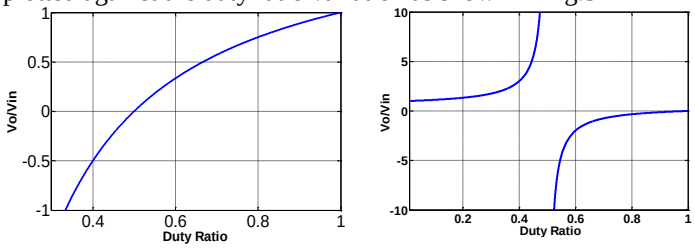

Fig.2. dc-dc converters with bidirectional output voltages: (a) and (b) voltage-buck converters, (c) and (d) voltage-boost converters.

The voltage conversion ratios of the converters can be expressed as:

$$M(D) = \frac{2D-1}{D} \quad for \quad b1G \quad and \quad b2G \quad (3)$$

$$M(D) = \frac{1-D}{1-2D} \quad for \quad B1G \quad and \quad B2G \quad (4)$$

The voltage conversion ratios in equations (3) and (4) can be plotted against the duty ratio variation as shown in Fig.3

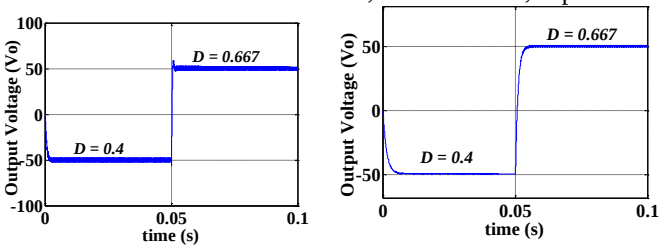



(a) b1G and b2G (b) (a) B1G and B2G

Fig.3. Voltage conversion ratios (M) versus duty ratio (D)

B1G and B2G have a discontinuous voltage ratio over the full operating range and cannot generate zero output voltage ($V_o$ = 0). However, b1G and b2G have continuous voltage ($V_o/V_{in}$) versus the duty ratios.

MATLAB simulation is shown in Fig. 4 at different duty ratios to show the buck converters, b1G and b2G, capabilities.

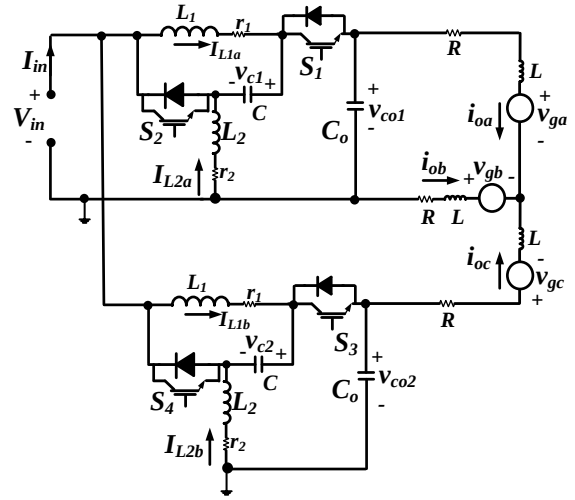



(a) b1G (b) (a) b2G

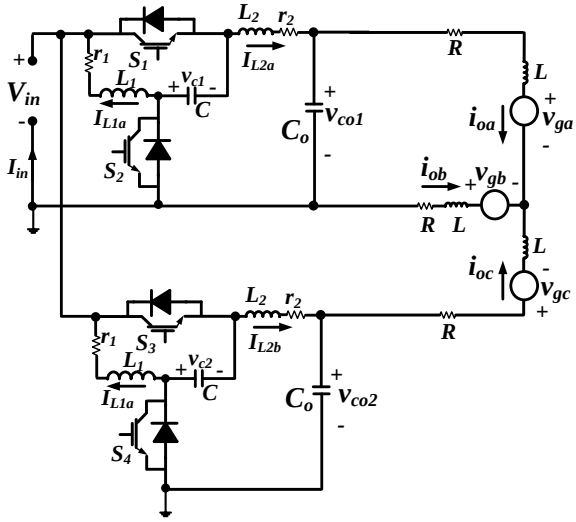
Fig. 4. Performance of buck converters *($V_{in}$ = 100V, C = 1μF, $C_o$ = 10 μF, $L_1$ = $L_2$ = 1mH, $t_s$ = 33μs, and load = 5Ω)*

## III. FOUR-SWITCH THREE-PHASE INVERTERS

Two converters can be connected deferentially across the three-phase load to form a FSTP inverter. The circuit diagrams of these inverters are shown in Fig. 5.




(a) b1G FSTP inverter




(b) b2G FSTP inverter

Fig. 5. Proposed FSTP inverters

Each converter produces sinusoidal voltage with peak $V_m$ as follows:

$$\begin{aligned} v_{co1}(t) &= V_m \sin(\omega t + \theta) \\ v_{co2}(t) &= V_m \sin(\omega t + \theta + \tfrac{1}{3}\pi) \end{aligned} \tag{5}$$

The output three-phase voltage can be expressed as:

$$\begin{aligned} v_{ga}(t) &= V_g \sin \omega t \\ v_{gb}(t) &= V_g \sin(\omega t - \tfrac{2}{3}\pi) \\ v_{gc}(t) &= V_g \sin(\omega t + \tfrac{2}{3}\pi) \end{aligned} \tag{6}$$

Where $\omega = 2\pi f$ is the angular frequency. This causes the three-phase currents $i_{oa}$, $i_{ob}$ and $i_{oc}$ to flow in the load as follows:

$$\begin{aligned} i_{oa}(t) &= I_o \sin \omega t \\ i_{ob}(t) &= I_o \sin(\omega t - \tfrac{2}{3}\pi) \\ i_{oc}(t) &= I_o \sin(\omega t + \tfrac{2}{3}\pi) \end{aligned} \tag{7}$$

Where:

$$\theta = \tan^{-1}\left\{\begin{array}{l} RI_o\left(\tfrac{3}{2}\sin(\gamma) + \tfrac{\sqrt{3}}{2}\cos(\gamma)\right) + \\ \omega L I_o\left(\tfrac{3}{2}\cos(\gamma) - \tfrac{\sqrt{3}}{2}\sin(\gamma)\right) + \tfrac{\sqrt{3}}{2}V_g \\ \hline RI_o\left(\tfrac{\sqrt{3}}{2}\cos(\gamma) - \tfrac{\sqrt{3}}{2}\sin(\gamma)\right) - \\ \omega L I_o\left(\tfrac{\sqrt{3}}{2}\sin(\gamma) + \tfrac{\sqrt{3}}{2}\cos(\gamma)\right) + \tfrac{3}{2}V_g \end{array}\right\} \tag{8}$$

$$V_m = \frac{\begin{array}{l} RI_o\left(\tfrac{\sqrt{3}}{2}\cos(\gamma) - \tfrac{\sqrt{3}}{2}\sin(\gamma)\right) - \\ \omega L I_o\left(\tfrac{\sqrt{3}}{2}\sin(\gamma) + \tfrac{\sqrt{3}}{2}\cos(\gamma)\right) + \tfrac{3}{2}V_g \end{array}}{\cos(\theta)} \tag{9}$$

The duty ratios of the converters $\delta_1$ and $\delta_2$ are calculated from (3) and (5) as:

$$\begin{aligned} \delta_1(t) &= \frac{V_{in}}{2V_{in} - v_{co1}(t)} \\ \delta_2(t) &= \frac{V_{in}}{2V_{in} - v_{co2}(t)} \end{aligned} \tag{10}$$

MATLAB simulations for the two converters open loop operations are shown in Fig. 6 and Fig. 7 using the components values in TABLE I.

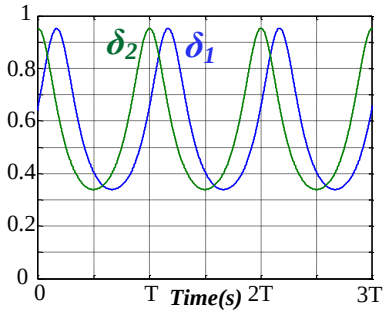
TABLE I. PARASITIC COMPONENT VALUES AND CIRCUIT CONDITIONS

| | |
|---|---|
| $f$ | 50 Hz |
| $t_s$ | 33 µs |
| $C$ | 1 µF (b1G) and 5 µF (b2G) |
| $C_o$ | 20 µF (b1G) and 1 µF (b2G) |
| $L_1$ | 1 mH |
| $L_2$ | 1 mH |
| $L$ | 1 mH |
| $R$ | 0.5 Ω |
| $r_1$ and $r_2$ | 0.05 Ω |
| $V_{in}$ | 100 V |

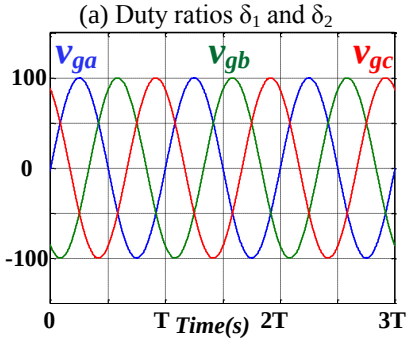
To study the dynamics of the buck converters, each one can be modelled and represented in its state space average model as follows:

### *a) b1G*

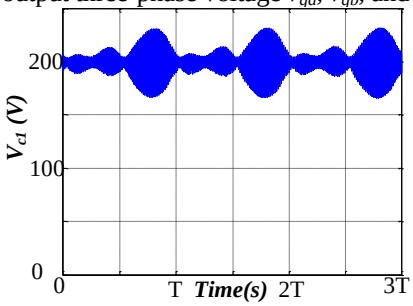
The circuit configurations of b1G converter are shown in Fig. 8, considering the inductors parasitic resistances ($r_1$, $r_2$) and the output inductance and resistance ($L$, $R$). The duration $t_{on}$ defines the period that either $S_1$ or its anti-parallel diode are coducting. The average model of b1G is expressed in (11). The poles map of b1G converter in Fig. 9 shows that the dynamics of the converter is changing with the small-signal duty ratio $\delta$.



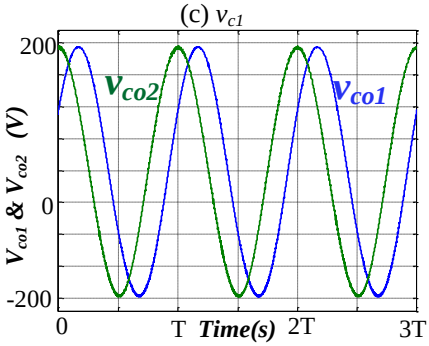

(a) Duty ratios $\delta_1$ and $\delta_2$



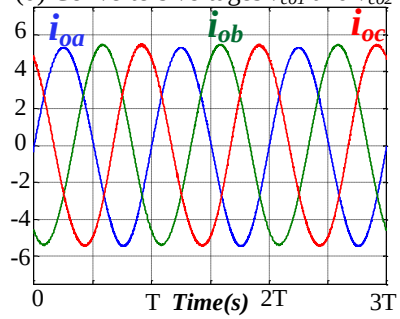

(b) output three-phase voltage $v_{qa}$, $v_{qb}$, and $v_{qc}$




(c) $v_{c1}$

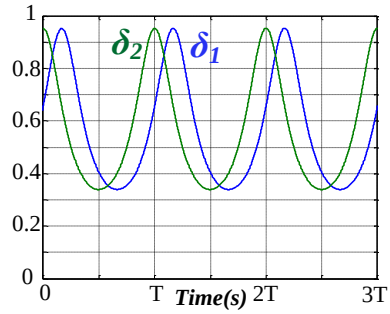



(d) Converters voltages $v_{co1}$ and $v_{co2}$

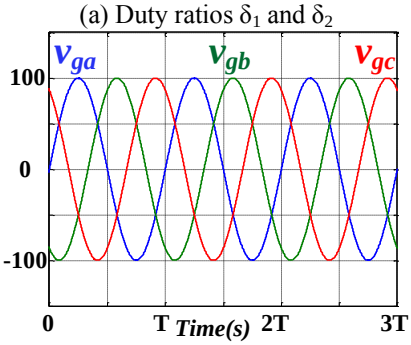



(e) output three-phase current $i_{oa}$, $i_{ob}$, and $i_{oc}$

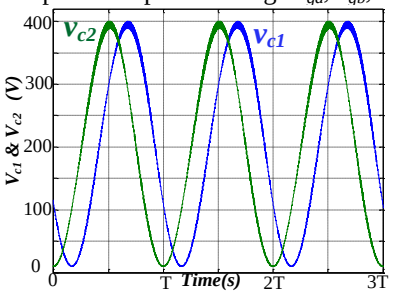
Fig. 6. Output voltages and currents of b1G FSTP inverter



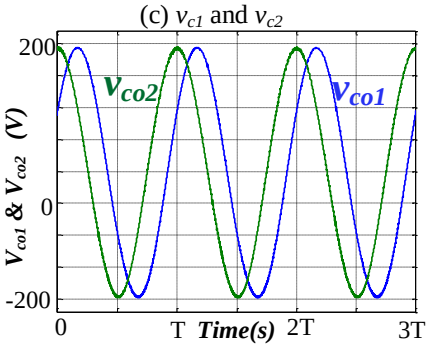

(a) Duty ratios $\delta_1$ and $\delta_2$



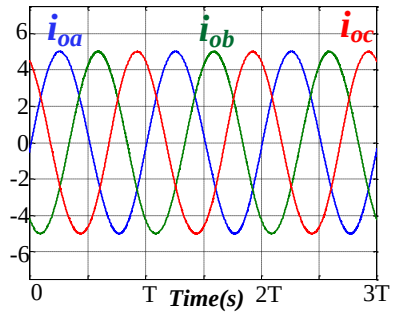

(b) output three-phase voltage $v_{qa}$, $v_{qb}$, and $v_{qc}$




(c) $v_{c1}$ and $v_{c2}$

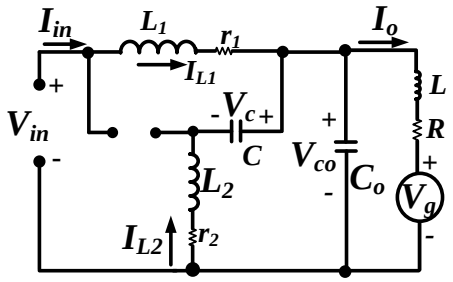



(d) Converters voltages $v_{co1}$ and $v_{co2}$

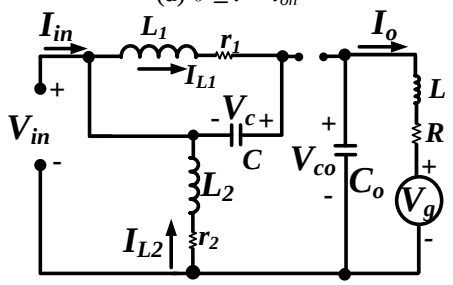



(e) output three-phase current $i_{oa}$, $i_{ob}$, and $i_{oc}$

Fig. 7. Output voltages and currents of b2G FSTP inverter




(a) $0 \le t < t_{on}$




(b) $t_{on} \le t < t_s$

Fig. 8. Configurations of b1G converter

$$\begin{bmatrix} \dot{I}_{L1} \\ \dot{V}_c \\ \dot{I}_{L2} \\ \dot{V}_{co} \\ \dot{I}_o \end{bmatrix} = \begin{bmatrix} \frac{-r_1}{L_1} & \frac{D-1}{L_1} & 0 & \frac{-D}{L_1} & 0 \\ \frac{(1-D)}{C} & 0 & \frac{-D}{C} & 0 & 0 \\ 0 & \frac{D}{L_2} & \frac{-r_2}{L_2} & \frac{-D}{L_2} & 0 \\ \frac{D}{C_o} & 0 & \frac{D}{C_o} & 0 & \frac{-1}{C_o} \\ 0 & 0 & 0 & \frac{1}{L} & \frac{-R}{L} \end{bmatrix} \begin{bmatrix} I_{L1} \\ V_c \\ I_{L2} \\ V_{co} \\ I_o \end{bmatrix} + \begin{bmatrix} \frac{D}{L_1} & 0 \\ 0 & 0 \\ \frac{D-1}{L_2} & 0 \\ 0 & 0 \\ 0 & \frac{-1}{L} \end{bmatrix} \begin{bmatrix} V_{in} \\ V_g \end{bmatrix} \quad (11)$$

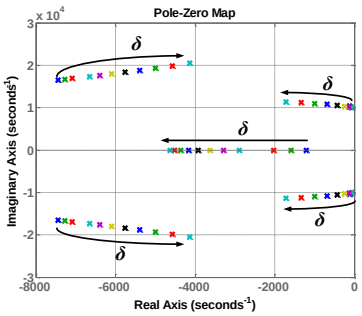
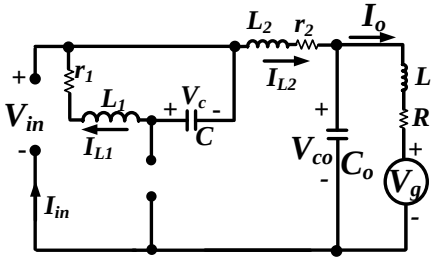



Fig. 9. Pole-zero map of b1G converter

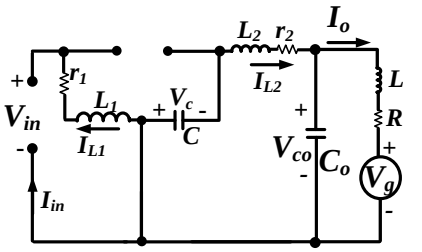
*b) b2G*

The circuit configurations of b2G converter are shown in Fig.10 . The average model of b2G is expressed in (12). Based on the average model, the pole loci map is shown in Fig.11.

Same as b1G, the poles move along specified trajectories representing the non-linear natures of these converters.




(a) $0 \le t < t_{on}$




(b) $t_{on} \le t < t_s$

Fig.10. Configurations of b2G converter

$$\begin{bmatrix} \dot{I}_{L1} \\ \dot{V}_c \\ \dot{I}_{L2} \\ \dot{V}_{co} \\ \dot{I}_o \end{bmatrix} = \begin{bmatrix} \frac{-r_1}{L_1} & \frac{D}{L_1} & 0 & 0 & 0 \\ \frac{-D}{C} & 0 & \frac{1-D}{C} & 0 & 0 \\ 0 & \frac{D-1}{L_2} & \frac{-r_2}{L_2} & \frac{-1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C_o} & 0 & \frac{-1}{C_o} \\ 0 & 0 & 0 & \frac{1}{L} & \frac{-R}{L} \end{bmatrix} \begin{bmatrix} I_{L1} \\ V_c \\ I_{L2} \\ V_{co} \\ I_o \end{bmatrix} + \begin{bmatrix} \frac{D-1}{L_1} & 0 \\ 0 & 0 \\ \frac{D}{L_2} & 0 \\ 0 & 0 \\ 0 & \frac{-1}{L} \end{bmatrix} \begin{bmatrix} V_{in} \\ V_g \end{bmatrix} \quad (12)$$

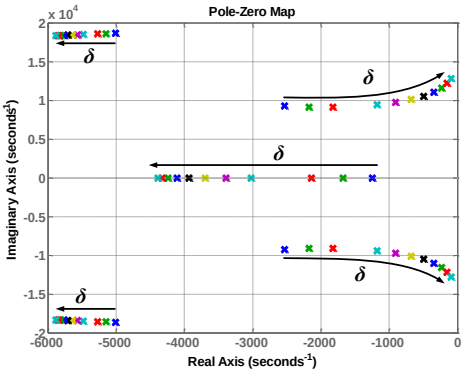



Fig.11. Pole-zero map of b2G converter

Because the proposed inverters are of high order systems, Variable Structure Control [15] (VSR) is an attractive solution. Sliding Mode Control (SMC) [15], which belongs to a family of VSR techniques, will be applied to the proposed inverters. The integral sliding mode controller for the proposed inverters is shown in Fig. 12.

Where $r_1$ and $r_2$ are the parasitic resistances of $L_1$ and $L_2$ respectively. $K_1$, $K_2$, $K_3$ are the gain values of the controller.

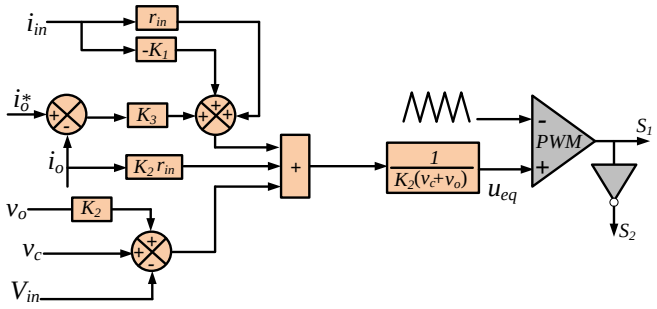



Fig. 12. Sliding mode controller of b1G FSTP inverter

## IV. THREE-SWITCH BUCK-BOOST SINGLE-PHASE INVERTERS

From the previous discussion, b1G and b2G converters can provide sinusoidal output for each leg. Consequently, each leg can form a single-phase inverter with two switches instead of four switches in the traditional voltage source inverter. However, the single-phase inverter suffers from 2nd order harmonic current component in the input side which creates higher current stresses, and hence higher power losses, as well as problems for the Maximum Power Point Tracking (MPPT) system if the inverter is implemented with PV systems. This can be solved if a boost converter is implemented with b1G and b2G resulting in a three-switch single-phase inverter as shown in Fig. 13. This inverter has important advantages as:

- Reduced power loss as one switch and one diode are removed
- Ability for 2nd order harmonic current decoupling
- Buck-boost voltage transfer function: this is an important feature when the inverter is implemented with PV systems where the input voltage might be lower or greater than the grid voltage.

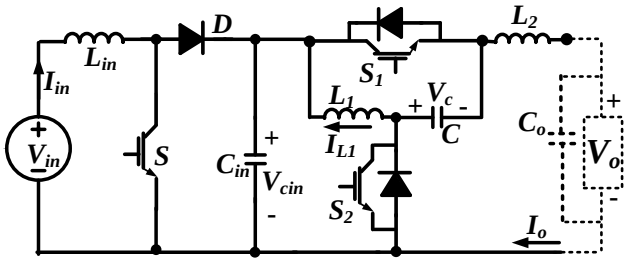
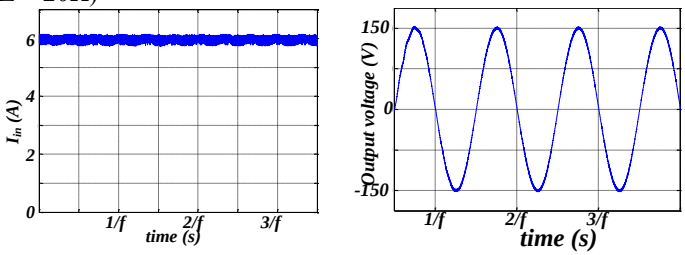
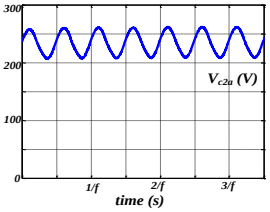



Fig. 13. Buck-boost single-phase b2G inverter

MATLAB simulation results in Fig. 14 show the closed loop operation when it is required to boost the input voltage ($V_{in}$) from 100V to a sinusoidal output voltage ($V_o$) of 150V peak. The input current $I_{in}$ is kept constant while the 2nd order power component is decoupled by the capacitor $C_{in}$. ($C_{in}$ = 200µF and Z = 20Ω)




(a) Input current $I_{in}$ (b) Output voltage ($V_o$)



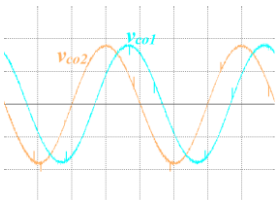

(c) intermediate capacitor voltage ($V_{cin}$)

Fig. 14. Simulation results of the inverter in Fig. 13.

An important feature of the proposed inverters in Fig. 13 is that the input current $I_{in}$ is continuous due to the existence of an input inductor in the dc side. This mitigates the need for input electrolytic dc capacitor across the dc input side. Mitigating the electrolytic capacitors increases the reliability of the inverter to great extent [16].

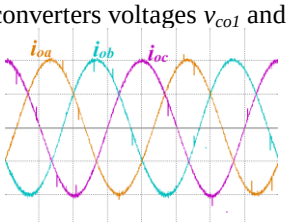
## V. EXPERIMENTAL RESULTS

The system concept, presented mathematical analysis and simulations are validated with b1G FSTP inverter using the parameters in Table I and controlled using a TMS320F280335 DSP. The DC input voltage ($V_{in}$) is fed from Sorensen SG A250X-10kW DC power supply. Four IRFPS40N60K MOSFET switches have been employed for the switches $S_{1\to4}$ with their freewheel diodes. $D_{1\to4}$. Clairtronic CMV-28F3, 0-415 V, 3–ph, auto-transformer is used to match the ac voltage grid. Fig. 15 shows the voltages and the currents of the proposed inverter.




(5ms/div – 100V/div)

(a) converters voltages $v_{co1}$ and $v_{co2}$




(5ms/div – 2.5A/div)

(b) three-phase output currents

Fig. 15. Experimental results for b1G FSTP

## VI. CONCLUSION

New dc-ac three-phase inverters with reduced number of switches are proposed in this paper. Reducing the switches number improves the efficiency and the reliability of the dc-ac inverters. The proposed three-phase inverters have greater maximum output peak voltages than the conventional FSTP. Unlike the conventional FSTP, the proposed inverters do not have dc bias in the converters' output voltages. However, the proposed inverters are high order systems where the poles of their transfer functions move with duty ratios variation. Consequently, the classical control strategies are not easy to be implemented. Sliding mode controllers for these inverters are proposed in order to generate pure sinusoidal voltages and currents. The paper presented as well new single-phase dc-ac inverter topologies with the ability to decouple the $2^{nd}$ order harmonic components from the input dc side.

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