A High-Gain, High-Voltage Pulse Generator using Sequentially-Charged Modular Multilevel Converter Sub-Modules, for Water Disinfection Applications

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***Abstract*– Modularity, redundancy and scalability are the key features recently sought in High-Voltage (HV) pulse generators for electroporation applications. Such features are gained by utilizing Modular Multilevel Converter (MMC) Sub-Modules (SMs). In this paper, two arms of MMC Half-Bridge SMs (HB-SMs) are utilized for generating bipolar/unipolar HV pulses for disinfection process in water treatment applications. The HB-SM capacitors are charged sequentially from a low voltage dc input source via a resistive-inductive branch and a reverse blocking switch (which is turned ON/OFF at zero voltage/current conditions). The energy losses of the proposed capacitor charging technique are established mathematically as well as the charging time per SM-capacitor. Therefore, the proposed Sequential Pulse Generator (SPG) is able to generate high repetitive pulse rates with high efficiency regardless the HV level of the pulse. Different characterizations of bipolar rectangular pulses can be generated. The proposed topology is assessed by Matlab/Simulink platform and scaled down experimentation. The results establish the viability of the SPG topology for HV pulse generation for water disinfection applications.**

***Index Terms*– Electroporation, high-voltage, Modular Multilevel Converter (MMC), pulse generator, pulse electric field, water treatment.**

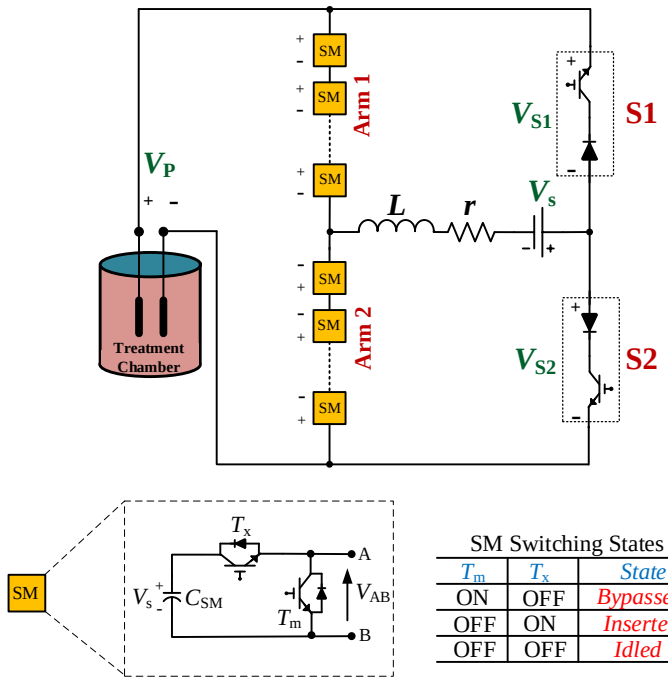
I. Introduction

CHLORINATION is commonly used for the disinfection process in water treatment applications [1]. Nevertheless, recent research established the effectiveness of applying Pulsed Electric Field (PEF) to disinfect water from harmful microorganisms (such as bacteria and E. coli) [2]. Successful disinfection is achieved by lethal electroporation; a process that produces electric pores in the biological cell membrane of the harmful microorganisms when subjected to High-Voltage (HV) pulses. The HV pulses are designed to create pores beyond a critical size at which the biological cell can reseal [3]. Typically, applying HV pulses of the kilo-Volt magnitude range (1-100 kV) with pulse durations ranging between nanoseconds and milliseconds is sufficient for lethal electroporation [4].

Among different pulse-waveform shapes, rectangular pulses are preferred, as they have an effective pulse plateau [4]. Generally, rectangular pulses are generated either in unipolar or bipolar shapes. Bipolar rectangular pulses are advantageous in terms of subjecting the microorganisms under treatment to reversing mechanical stress in addition to the electrical stresses [5].

HV Pulse Generators (PGs) generate HV pulses. Traditionally, HV pulse generation is obtained using Marx generators, pulse forming networks, and Blumlein lines [6]. However, these PGs are bulky, inflexible, and inefficient [7]. Therefore, PGs based on semi-conductor switches represent an excellent candidate for the classical generators. In solid-state Marx PGs, obtaining HV pulses usually exploits the feature of charging a number of capacitors in parallel, then connecting them in series (by means of semi-conductor switches) to discharge across the load, creating the required HV pulse [8]-[10]. Conventional Capacitor-Diode Voltage Multipliers (CDVMs) have been utilized in [11] to generate HV pulses across the load, while in [12], the CDVM stages are modified by adding Insulated Gate Bipolar Transistors (IGBTs) such that all capacitors discharge across the load, and higher output voltage can be obtained.

The inherited capacitors in the Modular Multilevel Converter (MMC) Sub-Modules (SMs) can be used for HV pulse generation. Generally, MMC-based PGs can be classified into two main categories: PGs with HVDC input and those with Low Voltage (LV) DC input. In HVDC-based PGs, the utilized MMC arms are rated at the HVDC level, as a result, balancing the individual SM capacitors to a certain voltage is crucial. Also, protection against short circuit at the HVDC level is required. In contrast, LVDC-based PGs mainly suffer from low repetition rates, and are primarily targeting rectangular pulse-waveforms. They may need additional bidirectional switches in junction with the MMC-SMs. Utilizing the MMC Half-Bridge SM (HB-SM) shown in Fig.1, is explored in several publications [7], [13]-[17].



SM Switching States

T_m	T_x	State
ON	OFF	*Bypassed*
OFF	ON	*Inserted*
OFF	OFF	*Idled*

Fig. 1. Proposed SPG topology.

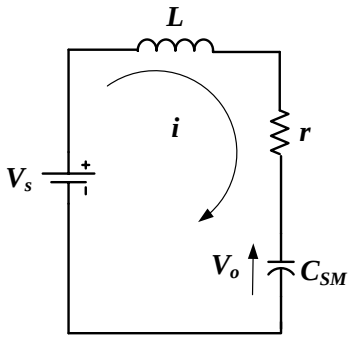


Fig. 2. Charging process equivalent circuit.

In [13]-[16], generating HV pulses is proposed using HVDC input supply. A common feature of these PG topologies is sensorless operation, where voltage balance of the SM capacitors is assured without any voltage measurements. In [13], a diode is added between the adjacent SMs, and with a proper switching of the individual SM IGBTs, voltage balancing is achieved. In [14], the capacitor voltage balancing is achieved through applying a specific modulation strategy to insert/bypass SMs. Although these techniques generate HV bipolar pulses, they only utilize half of the HVDC input voltage, and the operation deteriorates under SM failure. In contrast, in [15] an H-bridge, based on four arms of series-connected HB-SMs, is adopted. The pulse generation methodology assures sensorless SM capacitor voltages; operation under SM failure; and utilization of the full HVDC input, however, it requires a large number of SMs. In [16], with two HB-SM arms and two series-connected IGBT arms, forming an H-bridge fed from HVDC input, the SM capacitor voltages are measured and sorted continuously such that different pulse waveform shapes can be generated. In [7] and [17]-[18], a specific number of HB-SMs/Full-Bridge SMs (according to the required peak-pulse voltage) are charged sequentially from an LVDC input then discharged in series across the load, forming unipolar/bipolar HV pulses. But the charging mechanism is achieved via a relatively high charging resistances. Thus, the capacitors' charging time is elongated, which limits the generated repetition rate and/or the number of utilized SMs.

This paper proposes a bipolar HV PG fed from an LVDC input, based on the HB-SMs shown in Fig. 1. The proposed topology consists of two arms of series-connected HB-SMs, such that one arm, Arm1, generates a positive rectangular pulse polarity and the other arm, Arm2, generates a negative rectangular pulse polarity.

The SM-capacitors in each arm are charged sequentially from an LVDC input supply via a resistive-inductive (rL) branch through a reverse blocking switch formed of an IGBT connected in series with a diode. The reverse blocking switch has a Zero-Voltage Switching (ZVS) at turning ON and a Zero-Current Switching (ZCS) at turning OFF. The efficiency of the adopted capacitor charging technique is proved mathematically to be controlled via the voltage-drop across the SM capacitors. Moreover, the individual SM-capacitor charging time is deduced. Therefore, the proposed Sequential PG (SPG) is able to generate high repetitive pulse rates with reduced energy loss and shorter charging time per SM-capacitor. Different characterizations of bipolar rectangular pulses can be generated, namely pulses:

- with/without combined periods of positive and negative Null Load Voltage (NLV),
- with different positive and negative voltage-peaks, and
- with different positive and negative durations.

Additionally, the required SM capacitance is small, leading to a reduced converter footprint. Although bipolar rectangular pulses are the main target of the proposed topology, it can be modified for unipolar pulse generation by utilizing only one arm of series HB-SMs of the desired polarity. Table I summarizes the key features of the proposed PG in comparison with MMC-based PGs.

The validity of the proposed SPG converter is assessed via Matlab/Simulink simulations in addition to scaled-down experimentation. Results validate the proposed topology for water disinfection applications.

TABLE I
SUMMARY OF THE KEY FEATURES OF MMC BASED PULSE GENERATORS

		MMC based PG Topologies							
		[13]	[12]	[11]	[14]	[7]	[17]	[18]	Proposed SPG
Key Features	**Input voltage**	HVDC				LVDC			
	Input DC voltage utilization	100%	50%	50%	100%	N ×100%	N ×100%	N ×100%	N ×100%
	Topology description	Four arms of HB-SMs forming an H-bridge, switched ON/OFF simultaneously and SM-capacitors clamp the voltage across SM IGBTs	Phase leg of HB-SMs is switched via PWM technique following the desired wave-shape reference	Phase leg of HB-SMs is controlled via a specific balancing algorithm	An H-bridge formed of two HB-SMs and two arms of series-connected IGBTs that operate under ZVS conditions	N series connected HB-SMs that are charged sequentially from LVDC via a resistor	$2N$ series-connected HB-SMs that are charged sequentially from ±LVDC via a resistor	N series connected FB-MMC SMs that can charge sequentially from LVDC via a resistor	$2N$ series-connected HB-SMs are charged sequentially from ±LVDC via a resistive-inductive branch
	Capacitor voltage balancing control	Required and sensorless			Required, via voltage sensors	Not required. Attained automatically			
	Bipolar/Unipolar	Possible without physical changes to topology	Possible with physical changes to topology	Possible with physical changes to topology	Possible without physical changes to topology	Only unipolar pulses	Possible without physical change to topology		
	Switches utilized rather than MMC IGBTs	Not needed		Diode between any two adjacent SMs for capacitor voltage balancing	Series-connected IGBTs that operate with ZVS. Not necessarily the same number of the MMC arm SMs	Series connection of diodes to bypass the load during charging. In addition to two IGBTs to allow SMs charging and discharging	Two thyristors to bypass the load at charging, and four IGBTs to direct the charging current	Thyristor to bypass the load during charging. In addition to two IGBTs to allow SMs charging and discharging	Two reverse blocking switches operate with ZVS/ZCS conditions
	Repetition rate flexibility	Limited by controller speed	Limited by carrier frequency	Limited by balancing algorithm	Limited by controller speed and voltage sensor bandwidth	Limited by SMs charging time			
	Operation under SM failure	Possible without affecting the output pulse-peak, but voltage stresses increases across the failed SM arm	Not possible. Failure of one SM causes capacitor voltage imbalance		Possible without affecting output pulse-peak, but voltage stresses will increase across failed SM arm	Possible, but the output pulse-peak is reduced by the number of failed SMs No extra voltage stresses are expected			
	Scalability	Dependent on the HVDC input level				Dependent on the number of utilized SMs			

II. SPG TOPOLOGY AND OPERATING PRINCIPLE

The proposed SPG topology, shown in Fig. 1, is comprised of a combination of two series-connected HB-SM arms (Arm1 and Arm2) and two series-connected IGBT-diode switches (S1 and S2). Each HB-SM in Arm1 and Arm2 has a capacitor C_{SM} in series with an auxiliary IGBT/diode T_x, and both are paralleled to a main IGBT/diode T_m. Each SM can operate in any of three switching states; bypass, insertion and idle, as shown in Fig. 1.

The arrangement of SMs and series IGBT-diode switches (S1 and S2) is such that the individual capacitors of the upper N series-connected SMs, Arm1, are charged to $+V_s$ through S1 from input supply V_s. In contrast, the individual capacitors of the lower N series-connected SMs, Arm2, are charged through S2 from the same input supply V_s but in reverse polarity. The charging of each individual capacitor, either in Arm1 or Arm2, from the input supply is made sequentially via an rL circuit, as shown in the charging equivalent circuit in Fig. 2.

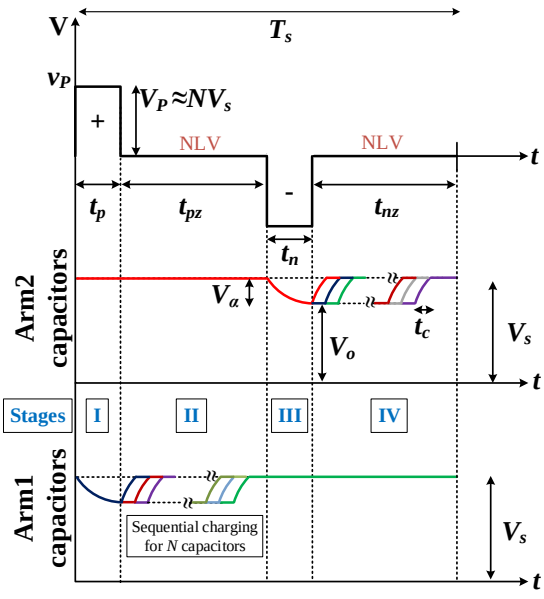


Fig. 3. SPG generated bipolar rectangular waveform and the corresponding charging/discharging sequence of Arm1 and Arm2 capacitors.

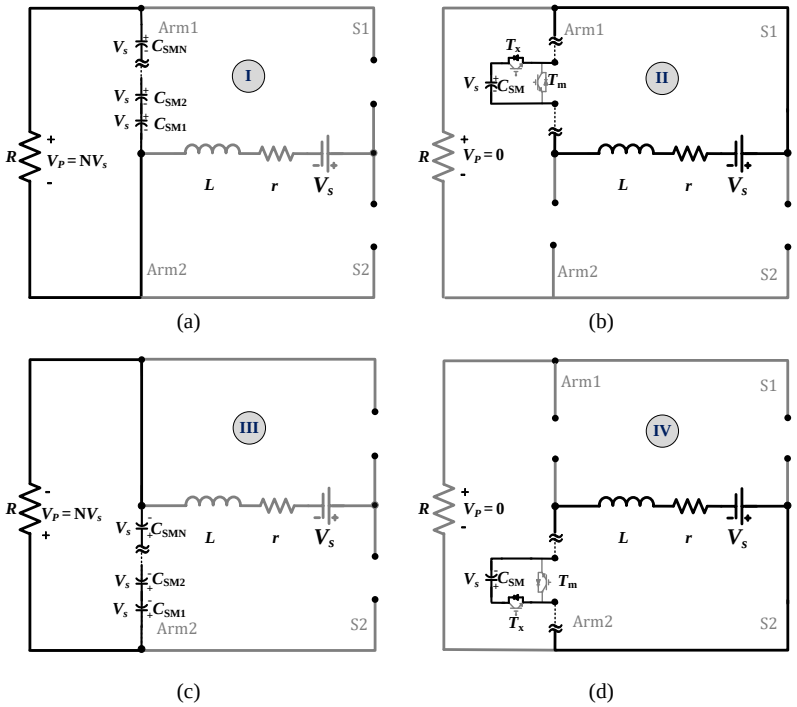


Fig. 4. SPG circuit configurations during bipolar pulse generation stages. (a) Stage I. (b) Stage II. (c) Stage III. (d) Stage IV.

Generating a bipolar rectangular pulse of peak voltage $V_P = \pm NV_s$, shown in Fig. 3, by the proposed SPG is achieved through the following stages (assuming all SM capacitors are pre-charged to V_s):

- *Stage I:* Arm1 SMs are inserted, and Arm2 SMs are bypassed, while the switches S1 and S2 are turned OFF as shown in Fig. 4a. Thus the load voltage is $+NV_s$ for the required positive pulse time t_p, and the supply V_s is disconnected.
- *Stage II:* after contributing to the positive pulse generation; in Arm1, each SM capacitor voltage decreases to V_o (as illustrated in Fig. 3). Thus, in stage II each capacitor is charged to V_s sequentially. Arm1 and Arm2 are idled, while S1 and S2 are maintained OFF from stage I, then the first SM in Arm1 is inserted. Consequently, S1 is turned ON (hence, near ZVS is assured) and the charging process, for the charging time (t_c), starts. After t_c, the charged SM is bypassed and the next SM is inserted for charging, etc. After the charging of the last SM capacitor, S1 is turned OFF (hence, ZCS is assured), then the SM is bypassed. During the total charging time of the N sequentially-charged SMs, $t_{pz} = Nt_c$, the load voltage is nulled as shown in Fig. 4b.
- *Stage III:* for a negative pulse period t_n, a negative pulse of peak $-NV_s$ is formed across the load by inserting Arm2 capacitors, while bypassing Arm1 SMs, and maintaining S1 and S2 OFF as shown in Fig. 4c.
- *Stage IV:* similar to stage III, the negative NLV time $t_{nz} = Nt_c$ is employed to sequentially charge the N individual capacitors of Arm2 SMs through S2, see Fig. 4d, while imposing a zero voltage across the load. The same approach of turning ON/OFF S1 is repeated for S2 such that ZVS and ZCS are assured at S2 turn ON and OFF, respectively.

Since the positive and the negative arms of the series-connected HB-SMs are charged independently, generation of symmetrical, as in Fig. 3, as well as asymmetrical rectangular bipolar HV pulses is possible as shown in Fig. 5. As a result, the SPG allows flexible bipolar rectangular HV pulse generation in symmetrical and asymmetrical forms. In Fig. 5a symmetrical combined NLV durations pulse is shown when the pulse cycle starts with positive polarity. The asymmetry is not only in negative (t_n)/positive (t_p) pulse durations as in Fig. 5b, but also in negative (V_n)/positive (V_p) pulse magnitudes, as in Fig. 5c. Fig. 5d shows combining both asymmetries in a combined NLV pulse when the pulse cycle starts with negative polarity. As a result of pulse generation flexibility, if one or more of the SMs fails (then bypassed) the pulse voltage will be asymmetrical (in magnitude). In order to have the same energy content, the pulse width is increased as depicted in Figs. 5b and 5d.

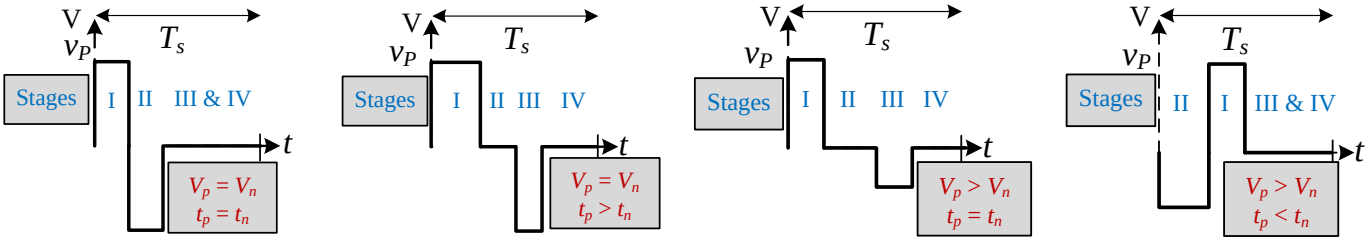


Fig. 5. Symmetrical and asymmetrical bipolar rectangular pulses. (a) Symmetrical combined NLV durations when the pulse cycle starts with positive polarity. (b) Duration asymmetry in bipolar rectangular pulses. (c) Magnitude asymmetry in bipolar rectangular pulses. (d) Asymmetrical combined NLV durations when the pulse cycle starts with negative polarity.

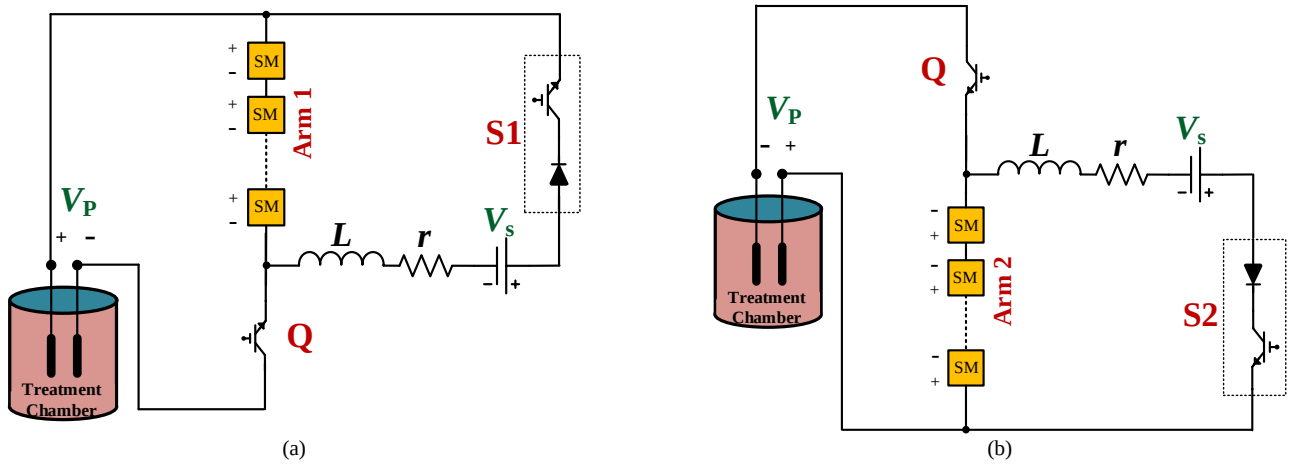


Fig. 6. Proposed SPG topologies for unipolar rectangular pulse generation. (a) Positive unipolar. (b) Negative unipolar.

For proper SPG operation, the IGBTs in the HB-SMs should be rated at the low voltage input dc supply V_s. Although, the IGBTs in S1 and S2 are rated at V_s, during positive and negative pulse generation, a reverse voltage of $(N-1)V_s$ is experienced across S1 and S2, respectively. Therefore a series diode to block such a voltage is necessary. Alternatively, any reverse blocking device, such as IGCT, can be utilized for S1 and S2 [19]-[20].

If unipolar pulses, with a specific polarity, are preferred using the topology in Fig. 1, the arm responsible for generating the other pulse polarity is disabled. However, it is more efficient and compact to replace the disabled HB-MMC arm with a single IGBT switch (Q) rated at V_s. Figs. 6a and 6b show the proposed unipolar SPG topologies for positive and negative HV pulse generation, respectively.

Load modeling depends on the duration of the applied pulses [21]. Basically, the sample under treatment is modelled by series resistor and capacitor, and is linearly related to the resistivity of the medium and its dielectric constant, respectively. For a pulse duration comparable to the dielectric relaxation time (which is typically in nanosecond order) of the medium, the capacitive component of the impedance can be neglected [21]-[23]. Thus, the load can be described by resistance (R), since the targeted range of pulse durations is in microseconds and higher, which are sufficient in water disinfection application.

III. Charging Process Analysis and SPG SM Capacitance Sizing

Consider the charging equivalent circuit in Fig. 2, where the SM-capacitor is initially charged to V_o such that $V_o < V_s$ and the resultant capacitor voltage drop due to the previous voltage pulse generation is $V_\alpha = V_s - V_o$. Applying KVL yields:

$$V_s = ri + L\frac{di}{dt} + \frac{1}{C_{SM}}\int i\,dt \tag{1}$$

Differentiate with respect to t and re-arrange terms

$$\frac{d^2i}{dt^2} + \frac{r}{L}\frac{di}{di} + \frac{i}{LC_{SM}} = 0 \tag{2}$$

To solve this second-order differential equation; two initial conditions are required. Since at re-charging, the initial current is zero:

$$i(0) = 0 \tag{3}$$

Also, the capacitor voltage is reduced to V_o, after discharging across the load during pulse generation, hence, at $t = 0$ applying KVL to find $\frac{di(0)}{dt}$,

$$ri(0) + L\frac{di(0)}{dt} + V_0 = V_s \tag{4}$$

Thus,

$$\frac{di(0)}{dt} = \frac{V_s - V_o}{L} = \frac{V_\alpha}{L} \tag{5}$$

TABLE II
RELATION BETWEEN r, L AND C_{SM} AND THE RESPONSE TYPE

Response type	Overdamped	Critically damped	Underdamped
Condition	$C_{SM} > \frac{4L}{r^2}$	$C_{SM} = \frac{4L}{r^2}$	$C_{SM} < \frac{4L}{r^2}$
Instantaneous current equation	$i(t) = A_1 e^{x_1 t} + A_2 e^{x_2 t}$	$i(t) = (A_1 + A_2 t)e^{-\alpha t}$	$i(t) = e^{-\alpha t}(A_1 cos\omega_d t + A_2 sin\omega_d t)$

Generally, the response of $i(t)$ depends on the roots of (2). The relation between r, L and C_{SM} that determines the response type and $i(t)$ mathematical expression are summarized in Table II. In Table II, A_1 and A_2 are constants to be calculated via the circuit initial conditions, $x_1$and x_2 are the roots of the differential equation, which are expressed as in (6).

$$x_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_o^2} \tag{6}$$

where $\alpha = \frac{r}{2L}$, $\omega_o = \frac{1}{\sqrt{LC_{SM}}}$ and $\omega_d = \sqrt{\omega_o^2 - \alpha^2}$.

A. Individual SM Capacitor Charging Efficiency

Since a critically damped response represents the margin between the other two response types, it is considered in the following analysis without loss of generality. The current $i(t)$ can be expressed as follows, while taking the initial conditions into account,

$$i(t) = \frac{V_\alpha}{L} t e^{-\alpha t} \tag{7}$$

The energy dissipated in r can be expressed as E_r where

$$E_r = r\int_0^\infty i(t)^2 dt = \frac{rV_\alpha^2}{L^2}\int_0^\infty t^2 e^{-2\alpha t}\, dt \tag{8}$$

The integration yields

$$E_r = \frac{rV_\alpha^2}{L^2}\left[\frac{-e^{-2\alpha t}(2\alpha^2 t^2 + 2\alpha t + 1)}{4\alpha^3}\right]_0^\infty \tag{9}$$

$$E_r = \frac{rV_\alpha^2}{L^2}\frac{1}{4\alpha^3} \tag{10}$$

Since $\alpha = \frac{r}{2L}$, (10) yields

$$E_r = \frac{rV_\alpha^2}{L^2}\left(\frac{8L^3}{4r^3}\right) = \frac{2L}{r^2}V_\alpha^2 \tag{11}$$

However, for a critically damped response type, $C_{SM} = \frac{4L}{r^2}$; substitution in (11) gives

$$E_r = ½C_{SM}V_\alpha^2 \tag{12}$$

The energy supplied E_s by the source V_s is

$$E_s = V_s\int_0^\infty i(t)dt = \frac{V_sV_\alpha}{L}\int_0^\infty te^{-\alpha t}\, dt \tag{13}$$

Integrating yields

$$E_s = \frac{V_sV_\alpha}{L}\left[\frac{-e^{-\alpha t}(\alpha t + 1)}{\alpha^2}\right]_0^\infty = \frac{V_sV_\alpha}{L}\frac{1}{\alpha^2} \tag{14}$$

Similarly, since $\alpha = \frac{r}{2L}$:

$$E_s = \frac{V_sV_\alpha}{L}\left(\frac{4L^2}{r^2}\right) = V_sV_\alpha\frac{4L}{r^2} \tag{15}$$

Again, for a critically damped response, $C_{SM} = \frac{4L}{r^2}$; substitution into (15) gives

$$E_s = C_{SM}V_sV_\alpha \tag{16}$$

The per unit (pu) charging inefficiency (η_{loss}) is expressed as

$$\eta_{loss} = \frac{E_r}{E_s} = \frac{½C_{SM}V_\alpha^2}{C_{SM}V_sV_\alpha} = \frac{½V_\alpha}{V_s} \tag{17}$$

Thus, the pu voltage drop determines the inefficient energy ($\%\eta_{loss}$) thus the charging energy efficiency ($\%\eta_{ch}$), as follows:

$$\%\eta_{loss} = 100 \times ½V_\alpha^{pu} \tag{18}$$

$$\%\eta_{ch} = 100 - \%\eta_{loss} \tag{19}$$

Regardless the response type (rC or under or over damped rCL), the inefficiency always dependant on the capacitor voltage drop. Inductance does not influence the efficiency, but affects the charging current peak and capacitor charging time.

B. Individual SM Capacitor Charging Time

Generally, for given initial conditions, the overdamped case has the longest charging time while the underdamped case has the fastest charging time. If a fast response, without severe oscillations or ringing, is desired, the critically damped case is used. In this paper, the response of the circuit is chosen to be underdamped with near unity damping factor. This provides a fast charging time with acceptable overshoot and negligible oscillation. The underdamped current is expressed as

$$i(t) = \frac{V_\alpha}{\omega_d L}e^{-\alpha t}sin\omega_d t \tag{20}$$

After charging the individual SM capacitor, the charging current is reduced to zero, hence, the actual charging time t_c^* can be calculated by setting $i(t_c^*) = 0$, solving (20) for t_c^* yields:

$$t_c^* = \frac{\pi}{\omega_d} \tag{21}$$

Accordingly, the software-controller assigned charging time, t_c, for each SM capacitor must be larger than t_c^* ($t_c > t_c^*$) such that the charging current drops to zero, therefore, assuring ZCS of the IGBT.

C. Individual SM Capacitor Sizing

The energy transferred to the resistive load per pulse polarity is expressed as [16]:

$$E_L = \frac{N^2V_s^2}{R}t_{pl} \tag{22}$$

TABLE III
SIMULATION AND EXPERIMENTAL SPECIFICATIONS

Parameter		Simulation	Experimental
LVDC input voltage	V_s	1 kV	200 V
Load pulse peak voltage	V_P	10 kV	600V
Input inductance	rL	1Ω and 2μH	2 Ω and 6μH
Number of SMs per Arm	N	10	3
Load resistance	R	1 kΩ	500 Ω
SM capacitance	C_{SM}	5 μF	5 μF
Assigned SM charging time	t_c	20 μs	60 μs
Repetition time	T_s	420 μs	400 μs
Percent remaining voltage	β	> 0.95	
Safety factor	γ	1.3	3.2

where E_L is the per pulse-polarity load energy and t_{pl} is the pulse-polarity duration. Accordingly, the load energy is transferred from the stored energy in the series inserted SM capacitors during pulse generation, hence

$$½NC_{SM}V_s^2(1-\beta^2) = \frac{N^2V_s^2}{R}t_{pl} \quad (23)$$

where β is the percentage remaining voltage on the SM capacitor after pulse generation. Thus, the SM capacitance is

$$C_{SM} = \frac{2Nt_{pl}}{(1-\beta^2)R} \quad (24)$$

To account for the neglected voltage drops across the semiconductor switches and parasitic resistances, a safety factor $\gamma \geq 1$ is introduced. Accordingly, the SM capacitance used in the proposed topology is selected based on

$$C_{SM} = \frac{2N\gamma t_{pl}}{(1-\beta^2)R} \quad (25)$$

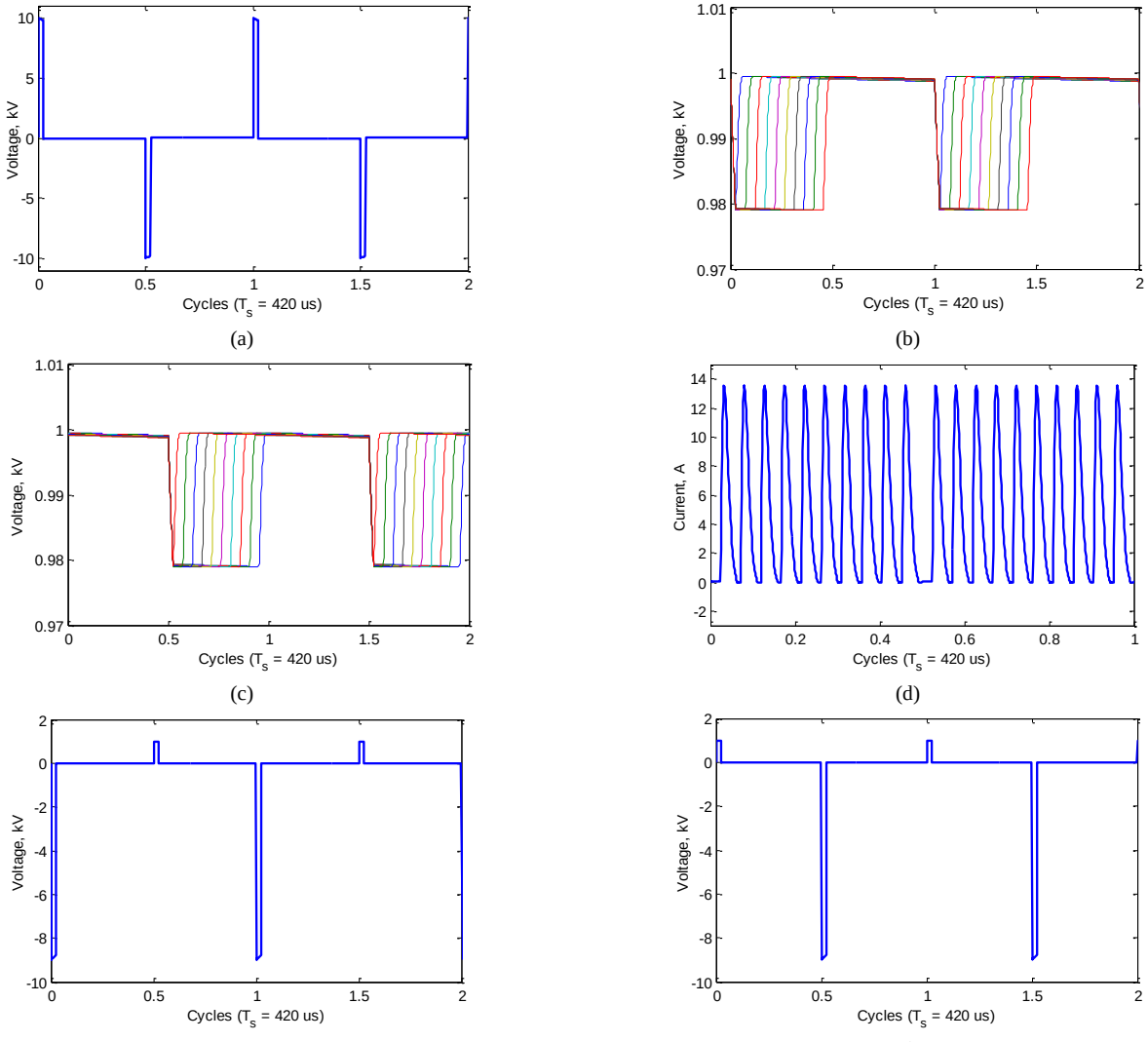


Fig. 7. Generation of 10 kV peak, 10μs symmetrical bipolar pulses. (a) Voltage pulses across the load. (b) Ten SM capacitor voltages of Arm1. (c) Ten SM capacitor voltages of Arm2. (d) Input charging current of the SM capacitors. (e) Voltage across S1. (f) Voltage across S2.

IV. Simulation Results

In order to assess the viability of the proposed SPG topology, Matlab/Simulink simulations are used, with the specifications in Table III.

With a 10µs pulse duration and 10 kV pulse peak, symmetrical bipolar voltage pulses are depicted in Fig. 7. The SM capacitors in Arm1 and Arm2 are charged through the rL branch sequentially to the LVDC supply level $V_s = 1$ kV. Fig. 7a shows the generated pulses across the load while Figs. 7b and 7c illustrate the charging and discharging sequence of the positive and negative SM capacitors, respectively. The input charging current for one cycle is shown in Fig. 7d, where the 20 SMs of Arm1 and Arm2 are charged sequentially in the positive and negative NLV periods, respectively. Based on the parameters in Table III, the individual SM capacitor charging current drops to zero after the charging time, $t_c^* = 16.2$ µs, as a result, in the software controller, the assigned charging time for each SM capacitor is set to $t_c = 20$ µs. Thus, after charging the last SM capacitor, switches S1 and S2 can be turned OFF safely at ZCS. The voltage stresses across S1 and S2 are shown in Figs. 7e and 7f.

Symmetrical combined NLV durations are shown with a positive pulse generated first and with a negative pulse generated first, with 10µs pulse duration and 10 kV pulse peak in Figs. 8a and 8b, respectively.

In Fig. 9, the generation of asymmetrical bipolar pulses is explored. Bipolar pulses with a positive peak of $V_p = 10$ kV and a negative peak of $V_n = 5$ kV with 10µs pulse duration for each polarity are shown in Fig. 9a. With 10 kV voltage peak, Fig. 9b shows bipolar pulses of positive pulse duration $t_p =$ 15µs and negative pulse duration $t_n = 5$µs. Combined NLV duration pulses of $V_p = 5$ kV, $t_p =$ 15µs, $V_n = 10$ kV, and $t_n = 5$µs are shown in Fig. 9c. The combined NLV duration pulses of $V_n = 4$ kV, $t_n =$ 15µs, $V_p = 5$ kV and $t_p = 5$µs are shown in Fig. 9d.

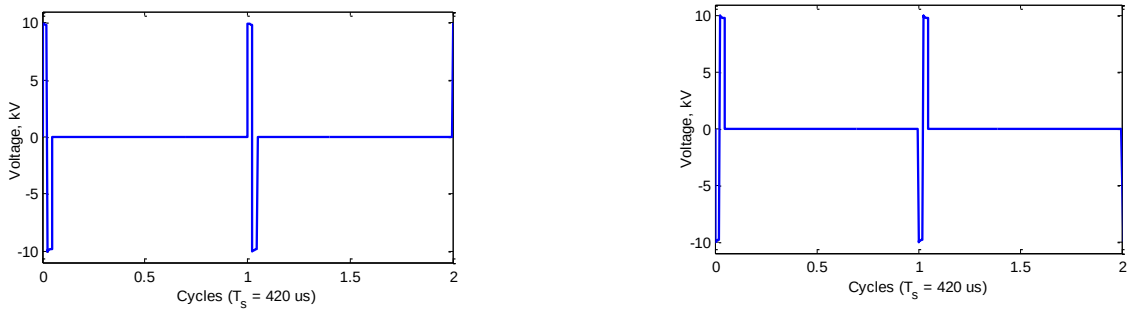


Fig. 8. Generation of 10 kV peak, 10µs symmetrical combined NLV durations bipolar pulses. (a) Positive pulse generated first. (b) Negative pulse generated first.

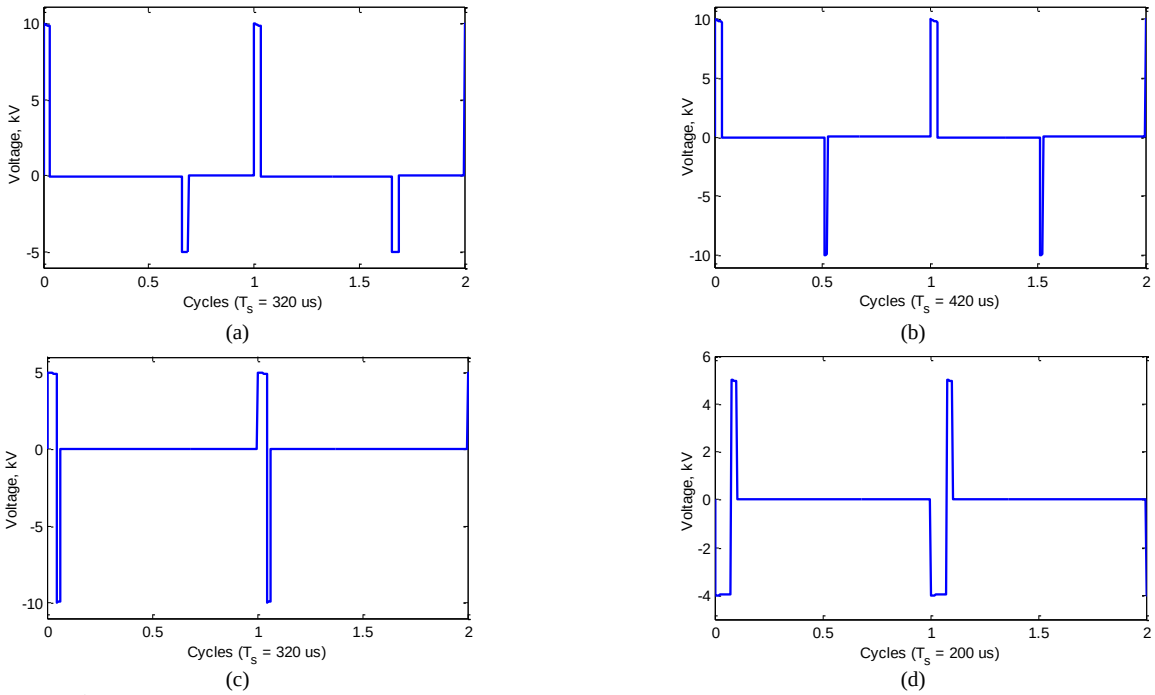
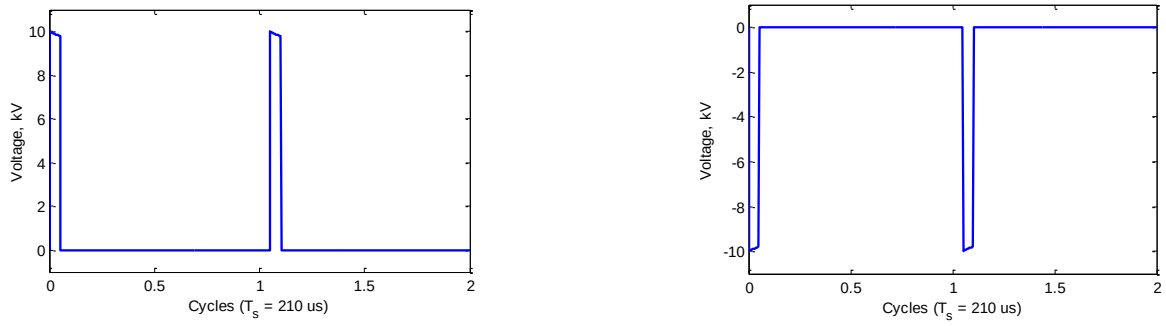


Fig. 9. Generation of asymmetrical bipolar pulses. (a) Positive and negative polarities magnitude asymmetry. (b) Positive and negative polarities duration asymmetry (c) Asymmetrical pulses with combined NLV durations when the pulse cycle starts with positive polarity. (d) Asymmetrical pulses with combined NLV durations when the pulse cycle starts with negative polarity.



(a) (b)

Fig. 10. Generation of 10 kV peak, 10μs unipolar pulses. (a) Positive pulse polarity. (b) Negative pulse polarity.

With the parameters in Table III and the unipolar SPG topologies illustrated in Fig. 6, unipolar pulses of peak voltage 10 kV, duration of 10 μs and repetition rate of $T_s = 210$ μs are generated are shown in Fig. 10. Fig. 10a shows unipolar pulses of positive polarity while Fig. 10b shows negative polarity unipolar pulses.

Table IV shows a quantitative comparison between the proposed SPG topology and the MMC-based sequential charging topologies using a charging resistor in [7], [17]-[18].

The comparison is based on generating HV pulses with a pulse peak voltage $V_P = 10$ kV, repetition time $T_s = 500$ μs (for unipolar mode $T_s = 250$ μs), and pulse duration time $t_{pl} = 20$ μs across a R = 1 kΩ resistive load. As shown in Table IV the capacitance in the sequential charging topologies in [7], [17]-[18] is 60% larger than for the proposed SPG topology. But the maximum current of the sequential charging topologies in [7], [17]-[18] is 23.3% lower than in the proposed SPG topology.

TABLE IV
QUANTITATIVE COMPARISON BETWEEN SEQUENTIAL CHARGING MMC-BASED PULSE GENERATORS

	Topology in [7]	**Topology in [17]**		**Topology in [18]**		**Proposed SPG Topology**	
Charging r/rL	$r = 3.6$ Ω	$r = 3.6$ Ω		$r = 3.6$ Ω		r =1.5Ω & L = 10μH	
SM Capacitance,	$C_{SM} = 6.43$ μF	$C_{SM} = 6.43$ μF		$C_{SM} = 6.43$ μF		$C_{SM} = 4$ μF	
Charging time/SM (t_c)♠	$t_c = 23$ μs	$t_c = 23$ μs		$t_c = 23$ μs		$t_c = 22.5$ μs	
Peak charging current	13.8 A	13.8 A		13.8 A		18 A	
Pulse Polarity	Unipolar	Bipolar	Unipolar	Bipolar	Unipolar	Bipolar	Unipolar
Repetition time (T_s)	250 μs	500 μs	250 μs	500 μs	250 μs	500 μs	250 μs
Number of SM/Arm	10	20	10	10		20	10
Type of SMs	Half-Bridge	Half-Bridge		Full-Bridge		Half-Bridge	
Number of Arms	1	2	1	1		2	1
Number of MMC IGBTs rated at LVDC	20	40	20	40		40	20
Number of switches other than MMC IGBTs, and their ratings	*Two IGBTs rated at LVDC	*Four IGBTs rated at LVDC.	*Two IGBTs rated at LVDC.	*Two IGBTs rated at LVDC.		*Two IGBTs rated at LVDC.	*Two IGBTs rated at LVDC.
	*One diode rated at HV pulse level (series connection of devices required).	*Two back to back thyristors rated at HV pulse level (series connection of devices required).	*One thyristor rated at HV pulse level (series connection of devices required).	*One thyristor rated at HV pulse level (series connection of devices required).		*Two Diodes rated at the HV pulse level (series connection of devices required).	*One Diode rated at HV pulse level (series connection of devices required).

♠ The charging time of the SPG must consider time for ZVS/ZCS conditions.

Furthermore, in the bipolar pulse generation mode, the proposed SPG can have the same repetition time as the unipolar pulse generator, where one of the upper and one of the lower SMs can be charged simultaneously, but at the expense of doubling the current drawn from the input supply. This feature is not possible in the PG topologies in [7], [17]-[18] due to their hardware structure.

V. Experimental Results

The scaled-down SPG power circuit of Fig. 1 uses IGBT switches (STGW30NC60WD) in the HB-MMC arms, which have antiparallel diodes, while switches S1 and S2 are comprised of (Infineon IGW60T120) IGBT in series with (IXYS DSEI30-10A) ultrafast power diode.

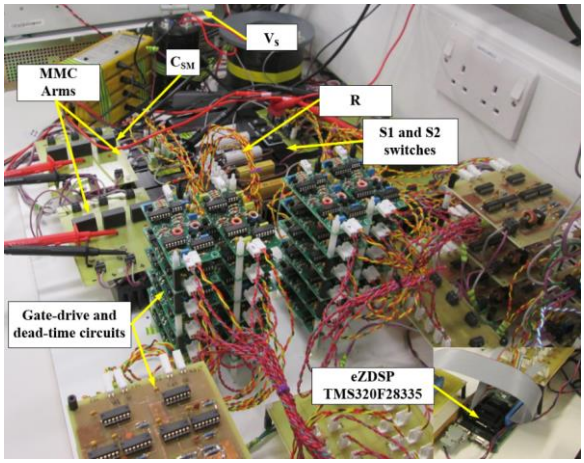


Fig. 11. The scaled-down experimental rig.

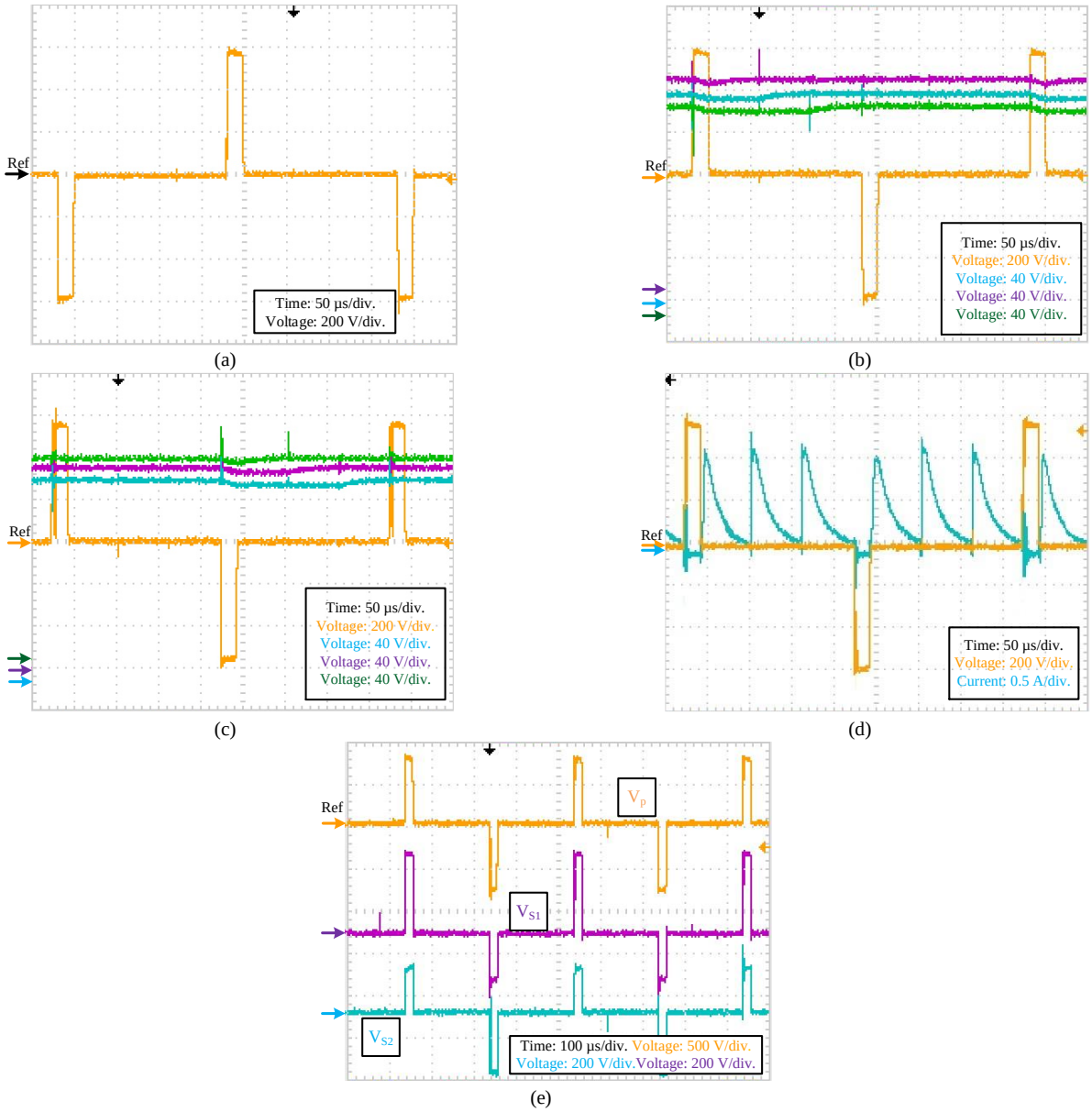


Fig. 12. Experimental generation of symmetrical bipolar pulses of 1.2 kV peak-peak. (a) Output voltage pulses. (b) Positive arm, Arm1, SM-capacitors voltage charging and discharging sequence. (c) Negative arm, Arm2, SM-capacitors voltage charging and discharging sequence. (d) Input charging current. (e) Voltage waveforms across switches S1 and S2.

The software algorithm was implemented in a Texas Instruments (TMS320F28335) DSP to generate the required gating signals for the SPG switches. The experimental specifications are given in Table III, and the scaled-down experimental rig is shown in Fig. 11.

Fig. 12 shows the generated symmetrical bipolar pulses with a peak-peak voltage of 1.2 kV, 20 µs pulse duration and $T_s = 400$ µs repetition rate. The generated voltage pulses are shown in Fig. 12a, while Figs. 12b and 12c show the charging and discharging sequence of the positive and negative arm SM-capacitors, respectively. In order to generate a peak voltage of 600 V per pulse-polarity, the individual SM capacitors are sequentially charged to the supply voltage $V_s =$ 200V. The input charging current is shown in Fig. 12d with assigned SM charging time $t_c = 60$ µs. The voltage waveforms across switches S1 and S2 (V_{S1} and V_{S2}, respectively) are depicted in Fig. 12e, measured as illustrated in Fig. 1.

During pulse generation each switch opposing to the inserted SM-capacitors is subjected to a reverse voltage of $V_P - V_s = 400$V, while the other switch is subjected to $V_s =$ 200V.

Generated asymmetrical bipolar pulses are shown in Fig. 13. 1.2 kV peak-peak, bipolar pulses of $t_p =$ 20 µs and $t_n =$ 10 µs are shown in Fig. 13a. Combined NLV durations bipolar pulses of $V_p = 600$V, $t_p = 10$ µs, $V_n = 200$ V and $t_n = 20$ µs are shown in Fig. 13b. Pulse duration of 20 µs combined NLV durations bipolar pulses of $V_p = 100$V and $V_n = 400$V are shown in Fig. 13c.

Unipolar pulses are generated by enabling the desired pulse polarity arm only, as shown in Fig. 14. Positive unipolar pulses are shown in Fig. 14a with a peak voltage of 600 V, pulse duration of 10 µs and repetition rate of $T_s = 190$ µs. Fig. 14b shows negative unipolar pulses with peak voltage of 600 V, pulse duration of 20 µs, and a repetition rate of $T_s = 200$ µs.

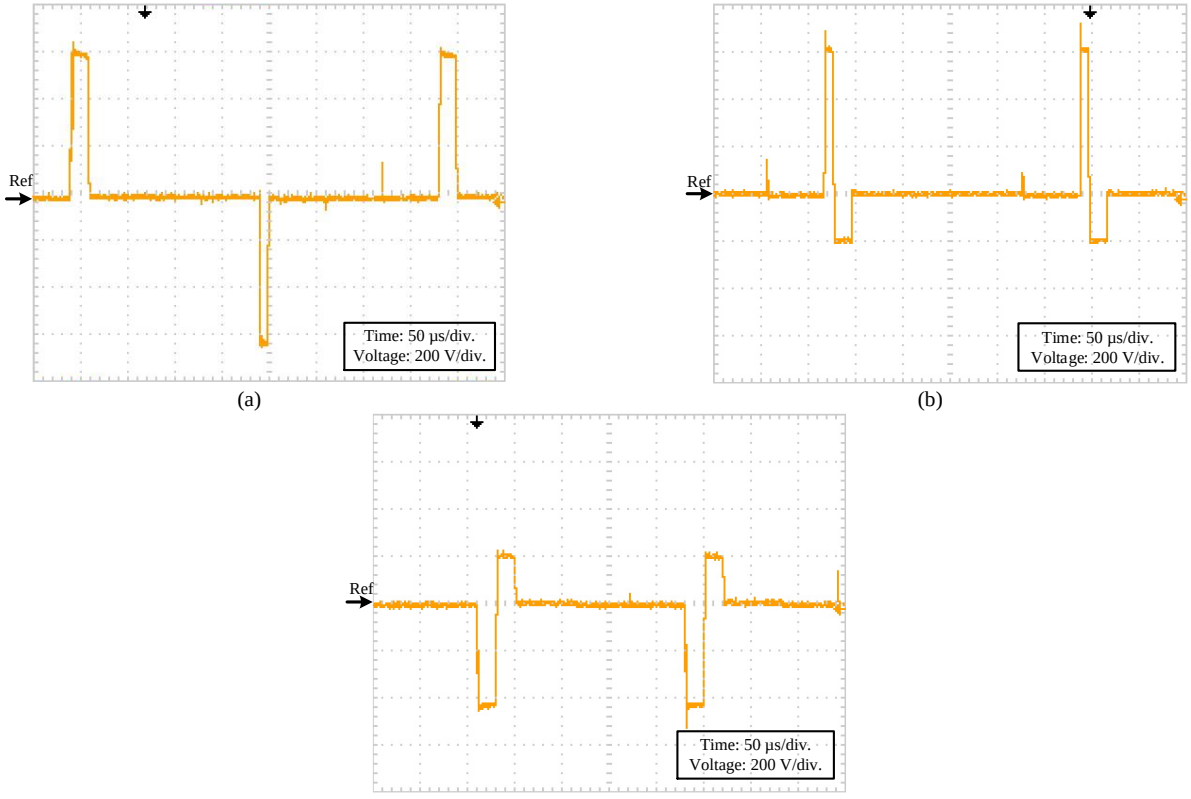
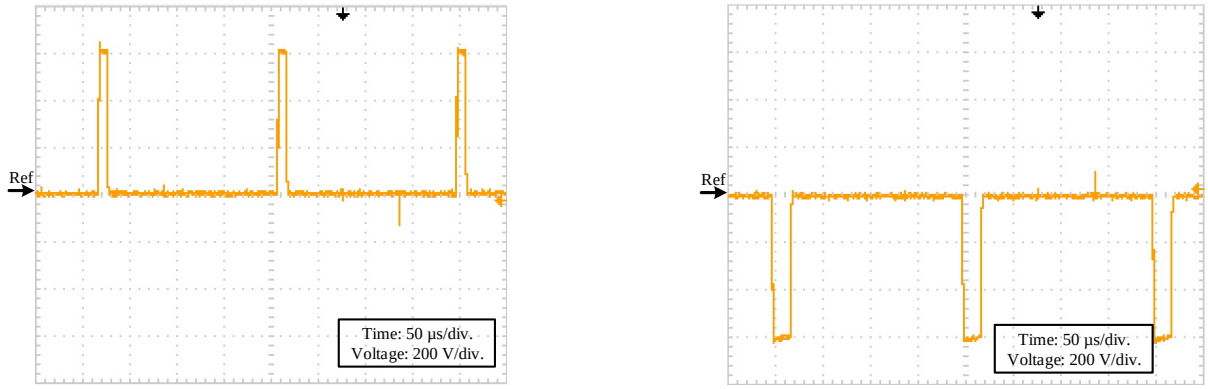


Fig. 13. Experimental generation of asymmetrical bipolar pulses. (a) Positive and negative polarities duration asymmetry. (b) Positive and negative polarities magnitude and durations asymmetry with combined NLV durations when pulse cycle starts with positive polarity. (c) Positive and negative polarities magnitude and durations asymmetry with combined NLV durations when the pulse cycle starts with negative polarity.



(a) (b)

Fig. 14. Experimental generation of 600V peak unipolar pulses. (a) Positive pulse polarity with 10 µs pulse duration. (b) Negative pulse polarity with 20 µs pulse duration.

VI. Conclusion

Complying with the emerging requirements of HV PGs such as redundancy, modularity, flexibility and scalability; this paper presented a new PG topology. The proposed PG topology is fed from an LVDC supply and the circuit configuration comprises two arms of series connected HB-SMs MMC (Arm1 and Arm2) in addition to two reverse blocking switches S1 and S2, forming an H-bridge. HV pulse generation is possible by sequentially charging the SM capacitors during the generated pulse null load voltage durations through a resistive-inductive branch and reverse-blocking switches (which turn ON/OFF at ZVS/ZCS conditions). The proposed SPG topology is able to generate HV bipolar rectangular pulses with flexible properties in magnitude and duration for both pulse polarities. The SPG mainly targets bipolar pulses, which have the merit of subjecting the sample under treatment to mechanical stresses and electrical stresses. Unipolar pulse generation is possible by deactivating the undesired pulse polarity arm. The capacitance size of the individual MMC-SMs is established to be small, in comparison to that a HB-MMC used in HVDC transmission applications; hence, the proposed converter has a smaller footprint. The efficiency of charging was proved mathematically to be controlled by the voltage-drop across the SM capacitors, due to conducting the pulse. The explored features of the proposed SPG topology via simulations and scaled-down experimentation, confirm the viability of the SPG for disinfection process in water treatment applications. The main contribution of the proposed SPG can be summarized as:

- It employs an LVDC input supply.
- It has the ability of generating unipolar/bipolar rectangular pulses with controllable voltage peak and duration.
- The number of sequentially charged SMs is a function of the required boosting ratio.
- It does not require voltage sensors.

The SM capacitors are charged from the LVDC supply via a resistive-inductive branch, which allows a controlled underdamped current to flow, and charges the capacitors swiftly, hence, higher repetitive rates are possible with controlled charging current peak.

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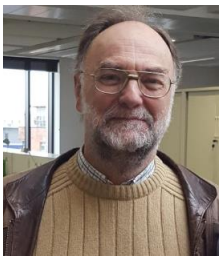

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