Review of DC Fault Protection for HVDC Grids

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Abstract

The development of modular multilevel converter (MMC) and the increased needs for long distance bulk power transmission using underground and subsea cables have promoted the rapid development and application of voltage source converter (VSC) based high-voltage DC (HVDC) systems. In this paper, recent advances in the area of DC fault protection in VSC based HVDC systems are reviewed. The main characteristics during DC faults are described and various converter topologies, which have DC fault blocking capability, are introduced and compared in terms of efficiency, cost, and control flexibility. The development of DC circuit breaker is introduced and various methods for DC fault detection and system level protection approaches for large scale HVDC grids are also discussed.

I. INTRODUCTION

For power transmission over long distance using cables, e.g. connection of large offshore wind farms, high-voltage DC (HVDC) has significant advantages compared to conventional AC technology due to the large reactive power consumption in AC cables [1]. HVDC also allows power transmission between unsynchronized AC systems. In addition, HVDC connections help increase system stability by preventing fault propagation and stabilize the predominant AC grid without increasing fault current level. HVDC also offers better active power controllability and can provide ancillary services for the connected AC grid, e.g. power flow redistribution, power swing damping, frequency stabilization, etc. [1-3]. A typical HVDC terminal contains the converter station, transformer, AC filters (if used) and associated control and protection equipment. For point-to-point transmission systems, the DC side of the HVDC terminal is connected to the DC side of the other terminal via cables or over-head-lines.

The rapidly developed voltage source converter (VSC) based HVDC systems during the past decade provide improved operation performance when compared to the traditional line commutated converter (LCC) based HVDC technology including flexible active and reactive power control, black start capability etc. This has further promoted the adoption of HVDC systems for connecting weak AC systems, island networks and renewable sources to main grids [4]. In recent years, modular multilevel converters (MMC) have become the chosen technology for future VSC based HVDC grids, due to their significant advantages over other two-level and three-level VSCs. Fig. 1 shows the schematic diagram of one MMC station, which has 6 converter arms each containing large numbers (usually a few hundred for HVDC systems) of half-bridge (HB) submodules (SMs) [5,6]. MMC can be easily adapted to higher voltage levels due to its modular design of the SMs, and the output voltages and currents of the MMC have negligible harmonics thus reducing/avoiding the use of AC side filters [4-6]. In addition, the switching frequency of MMC is typically in the range of one to two hundreds

Hertz leading to a much lower switching power losses compared to its two-level and three-level counterparts. Due to the small transient voltage step, potential electromagnetic interference issues are also largely avoided.
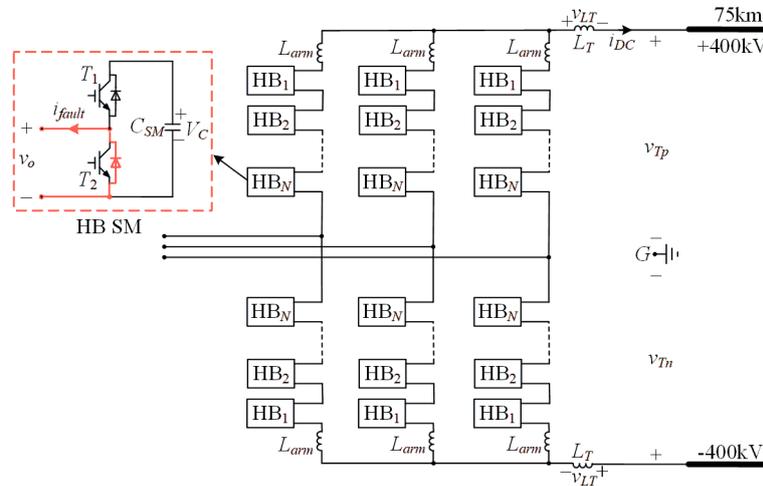

Fig. 1. Circuit of a HB-MMC.

DC fault protection is one of the most important challenges to the development of VSC based HVDC transmission systems. For unearthed DC systems or systems with high impedance grounding on the DC side, a pole-to-ground DC fault will not cause significant overcurrent but expose DC cables and converter transformers to DC voltage stresses. However, due to the low DC impedance, a DC pole-to-pole fault can result in the collapse of DC voltages within a few milliseconds and large AC and DC overcurrents flowing through the anti-parallel (freewheeling) diodes of the HB SMs, as shown in Fig. 1 even after the blocking of the converter (switching off all the IGBT devices). However, power electronics devices used in the MMCs have limited overcurrent capability and are vulnerable to the rapidly increased DC fault current. Thus, the protection speed required in DC grid needs be much faster than that in AC grid protection. In addition, the DC fault current does not have zero crossing point, which makes the breaking of DC fault current challenging.

AC circuit breakers (ACCBs) or DC circuit breakers (DCCBs) can potentially be used to disconnect the HB based MMC (HB-MMC) from the AC grid or DC fault point to interrupt the fault [7]. However, the response of ACCB is slow (typically in the range of several tens milliseconds) so the power electronics devices in the MMC will suffer high current stress during the fault period. For DCCBs, due to the need for fast interruption of large fault current, significant technical challenges have not been overcome and they are likely to be bulky and expensive [8, 9].
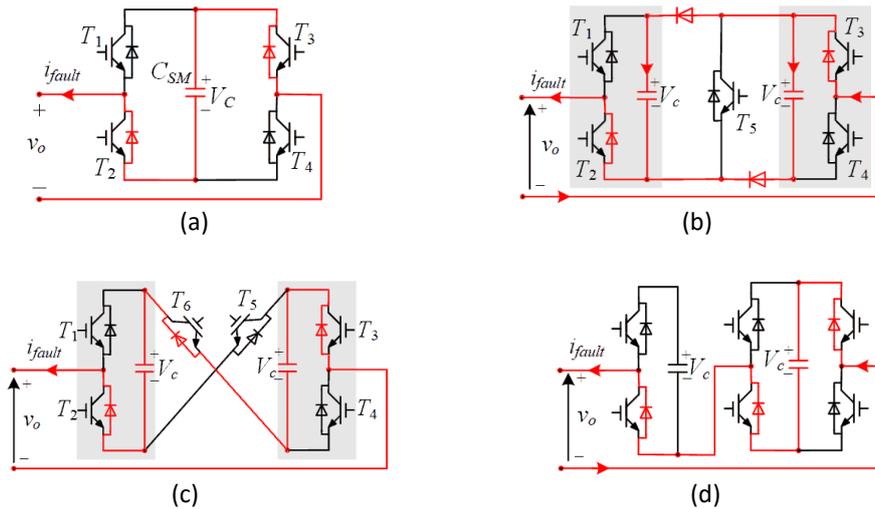
Fig. 2. Fault current path after the SMs are blocked: (a) FB [10, 11], (b) CD [12, 13], (c) CC [14], and (d) mixed SMs [15].

Based on the conventional HB SMs, various SM circuits as shown in Fig. 2 have been proposed which are capable of blocking fault current feeding from AC to DC in the event of a DC fault, e.g. full-bridge (FB) [10], clamped double (CD) [12, 13], cross connected (CC) [14], and mixed submodules [15], etc. After blocking the power devices in the SMs, i.e. IGBTs, following the fault, the SM capacitors in these topologies provide negative voltage to the AC fault current path, which then quickly suppresses the AC fault current to zero. However, such SMs with DC fault blocking capability require additional power electronics devices in the conduction path during normal operation, leading to extra conduction losses and capital cost.

Although the conventional HB-MMC cannot block DC faults, it has the minimum loss and capital cost compared to other MMC configurations. Passive and active fault current limiting methods in the DC network have been discussed to enable the HB-MMC to ride-through DC faults [16]. For a large multi-terminal HVDC system, in the event of a DC fault, it is desirable that the converters connected to the healthy DC lines continue operating without disruption while the faulty branches are quickly isolated. This raises the requirement of fast fault detection and faulty line identification [17].

The main objective of this paper is to provide an overview on the DC fault characteristic, fault detection and protection technologies of MMC based HVDC grid, and various fault blocking converter and DCCB configurations. The rest of the paper is organized as follows. Typical DC fault characteristics are described in Section II. Section III reviews various converter topologies with DC fault blocking capability. DC fault detection and protection approaches in the HVDC grid, and DCCB technologies are assessed in Section IV, and finally Section V draws the conclusions.

II. DC FAULT CHARACTERISTICS

A. Output Voltages of Half-Bridge SM

The typical circuit of the conventional HB-MMC has been illustrated in Fig. 1, considering N numbers of SMs are connected in series in each arm. Each HB SM has three switching states, as listed in Table I, where '1' and '0' indicate the relevant IGBT (T_1 or T_2) is switched ON and OFF respectively, and V_c is the SM capacitor voltage. In normal operation, a HB SM generates two voltage levels (0 and V_c) depending on the complementary switching states of T_1 and T_2.

After the occurrence of a DC fault, the MMC is blocked (i.e. all the IGBTs are switched off) but the fault current continues flowing through the antiparallel diodes in each HB SM into the DC fault, as illustrated by Fig. 1. Under such a condition, the conducting HB SM effectively outputs zero voltage. High fault currents are fed by the AC grid due to the low impedance in the fault current path until the MMC is either isolated from the fault on the DC side via DCCBs or disconnected from the AC grid by ACCBs [18].

TABLE I

Output Voltages of HB SM.

	Switching State	T_1	T_2	Output Voltage
Active	I	1	0	V_c
control state	II	0	1	0
Blocking	III	0	0	0 (when feeding fault current)

B. DC Fault Stages

According to the DC and/or AC components in the fault current, the fault process can be divided into three stages [16, 19].

1) Stage I

Taking a DC pole-to-pole fault as an example, at the initial stage of the fault, the MMC station can still generate the required AC voltage and the AC current can remain controlled [20]. However, as the station continues producing rated DC voltage while the DC voltage at the DC fault point is significantly reduced, this leads to a rapid increase of the DC component in the fault current, as illustrated in Fig. 3 (a). In the figure, C_u and C_l are the equivalent upper and lower arm capacitors respectively and the sum of their voltages (v_u and v_l) at Stage I of the fault remains largely at V_{DC}.
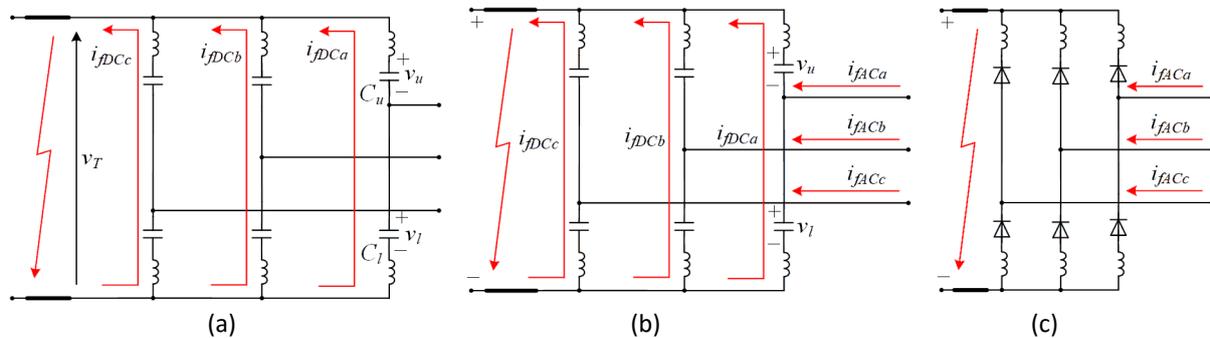

Fig. 3. Fault current behavior at different stages: (a) Stage I, (b) Stage II, (c) Stage III.

As illustrated in Fig. 3 (a), the three-phase DC circuits are connected in parallel as seen from the station terminal and contribute to the fault current. The fault current in Stage I largely contains only DC component as the converter AC current can still be controlled [16, 20].

2) Stage II

With the discharge of the SM capacitors and the reduction of the DC voltage, the converter starts to lose control of the AC current as the MMC cannot generate the required AC voltage. Thus, in addition to the DC component, AC fault current components start to appear in the arm which are fed by the grid voltage as shown in Fig. 3 (b) [16, 21-23], and the fault process moves to Stage II.

3) Stage III

The fault process moves to state III after the fault detection and subsequent blocking of the MMC converter during which the SM capacitors are bypassed. The grid continues feeding current to the DC fault through the antiparallel diodes of the HB SMs and the MMC acts as an uncontrolled diode rectifier, as illustrated by Fig. 3 (c) [24]. Depending on the fault detection speed, if the fault is detected in Stage I and the MMC is subsequently blocked, the fault process directly proceeds from Stage I to State III.

III. CONVERTER TOPOLOGIES WITH DC FAULT BLOCKING CAPABILITY

A. SM Structures with DC Fault Blocking Capability

As HB-MMCs do not have DC fault blocking capability, the fault current from the AC grid flows through the SM antiparallel diodes into the DC fault after the blocking of the MMC. This leads to higher AC and DC fault currents affecting both the MMC station and the AC and DC grid operation. To tackle this issue, various SM structures have been proposed to provide DC fault blocking capability [10, 12, 13, 15, 25].

1) Full-bridge (FB) submodules

By blocking all the switches T_1-T_4 in the FB SM shown in Fig. 2 (a), the capacitor C_{SM} is inserted into the conduction path in negative polarity to block the fault current flowing though the freewheeling diodes fed by the AC grid voltage. Alternatively, the FB based MMC (FB-MMC) can also continue operating during the fault (e.g. as a STATCOM) as the FB SMs can generate negative voltages, as listed in Table II, which offers greater controllability. However, FB-MMC doubles the required power electronics devices of that of HB-MMC, leading to additional losses in the conduction path compared to the equivalent HB arrangement [10, 11].

TABLE II
Output Voltages of Full-Bridge (FB) SM.

	Switching State	T_1	T_2	T_3	T_4	Output Voltage
Active control state	I	1	0	0	1	V_c
	II	0	1	1	0	$-V_c$
	III	1	0	1	0	0
	IV	0	1	0	1	0
Blocking	V	0	0	0	0	$-V_c$ (for DC fault blocking)

2) Clamped double (CD) submodules

To reduce the losses and number of required power devices, the clamped double (CD) submodule is proposed in [12, 13], as shown in Fig. 2 (b). In normal operation, switch T_5 is always switched ON, as listed in Table III. With the maximum voltage of $2V_c$, the CD SM generates five voltage level and is equivalent to two series-connected HB SMs. When a DC fault is detected, T_5 is switched OFF and the two capacitors are connected in parallel providing negative polarity voltage to the fault current path, as shown in Fig. 2 (b). Compared to that of its FB counterpart, the semiconductor number in the conduction path is reduced by 1/4, yielding reduced cost and conduction loss [12, 13]. However, the

CD SM only utilizes half of the possible SM capacitor voltages to block DC faults due to the two paths appeared in parallel.

TABLE III
Output Voltages of Clamped-Double (CD) SM.

	Switching	T_1	T_2	T_3	T_4	T_5	Output Voltage
Active control state	I	1	0	0	1	1	$2V_c$
	II	0	1	1	0	1	0
	III	1	0	1	0	1	V_c
	IV	0	1	0	1	1	V_c
Blocking State	V	0	0	0	0	0	$-V_c$ (for DC fault blocking)

3) Cross connected (CC) submodules

The cross connected (CC) SMs presented in [14] use additional two clamp switches T_5 and T_6 to connect two HB SMs and can generate $-2V_c$ by switching OFF both T_5 and T_6 to block the DC fault, as shown in Fig. 2 (c) and listed in Table IV. However, the two clamp switches T_5 and T_6 must be rated at twice the capacitor voltage thus the effective total number of switches required is the same as two FB SMs in addition to the need for series connection of two switches in the CC SM.

TABLE IV
Output Voltages of Cross Connected (CC) SM.

	Switching State	T_1	T_2	T_3	T_4	T_5	T_6	Output Voltage
Active control state	I	1	0	1	0	1	0	V_c
	II	1	0	1	0	0	1	$-V_c$
	III	1	0	0	1	1	0	$2V_c$
	IV	1	0	0	1	0	1	0
	V	0	1	1	0	1	0	0
	VI	0	1	1	0	0	1	$-2V_c$
	VII	0	1	0	1	1	0	V_c
	VIII	0	1	0	1	0	1	$-V_c$
Blocking	IX	0	0	0	0	0	0	$-2V_c$ (for DC fault blocking)

4) Mixed submodules

The mixed SM presented in [15] connects a FB SM with a HB SM in series to obtain DC fault blocking capability and reduce losses, as shown in Fig. 2 (d). It can generate negative voltage ($-V_c$), which allows the converter to block the DC fault and offers greater controllability than the HB SM.

The mixed SM is equivalent to the so-called hybrid MMC where the FB and HB SMs are mixed in each arm in the converter with their ratio fixed at 1. In [24], this ratio is greater than one in order to transfer more power than the conventional MMC by utilizing the negative output voltage capability of the FB SMs. However, with more HB SMs replaced by FB SMs, the conduction losses are increased.

5) Unipolar submodule structures

In addition to positive and zero voltage levels, the aforementioned FB [10], CC [14], and mixed SMs [15] can generate negative voltages in active control mode and offer more control flexibilities. Another alternative is the unipolar circuits, as shown in Figs. 4 (a)-(c), which do not have negative

voltage generating capability during operation but can still provide negative voltage to block AC fault current from feeding the DC fault. As shown in Fig. 4 (a), the unipolar FB SMs use one less IGBT compared to its bipolar FB counterpart shown in Fig. 2(a), yielding reduced semiconductor cost. The unipolar CC and mixed SMs can be derived in a similar way, as shown in Figs. 4 (b) and (c) respectively [26, 27]. The CD SM cannot generate negative voltage so belongs to the unipolar SM category but uses one more diode compared with the unipolar mixed SM shown in Fig. 4 (c).
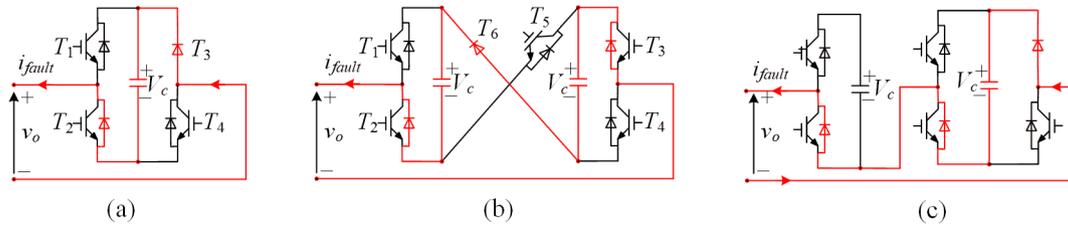

(a)   (b)   (c)

Fig. 4. DC fault current path of unipolar submodule circuits: (a) unipolar FB SM, (b) unipolar CC SM, and (c) unipolar mixed SM [26, 27].

B. Hybrid Cascaded Multilevel Converters

Recently, many other 'Hybrid Converter' configurations have been proposed which combine different topologies in order to optimize converter performance.

1) Alternate arm converter (AAC)

Based on conventional 2-level converter and FB-MMC, the alternate arm converter (AAC) is presented in [28-31], where each arm is composed of series connected FB SMs and a direct high voltage switch, as illustrated in Fig. 5 (a). The upper and lower arms are alternatively connected in the conduction path by the direct switches to generate positive and negative half-cycles of the AC voltage. Thus, the required FB SM number is reduced to around half of that of a full FB-MMC, yielding reduced semiconductor losses while the DC fault blocking capability is retained. To ensure full AC voltage operation range, extended overlap operation of AAC [32-34] is usually used which also eliminates potential 6th harmonic in the DC current [30, 34-36]. However, this leads to higher AC terminal to ground voltage stress [32]. In addition, the direct switches in the AAC arm require series connection of large numbers of IGBTs.
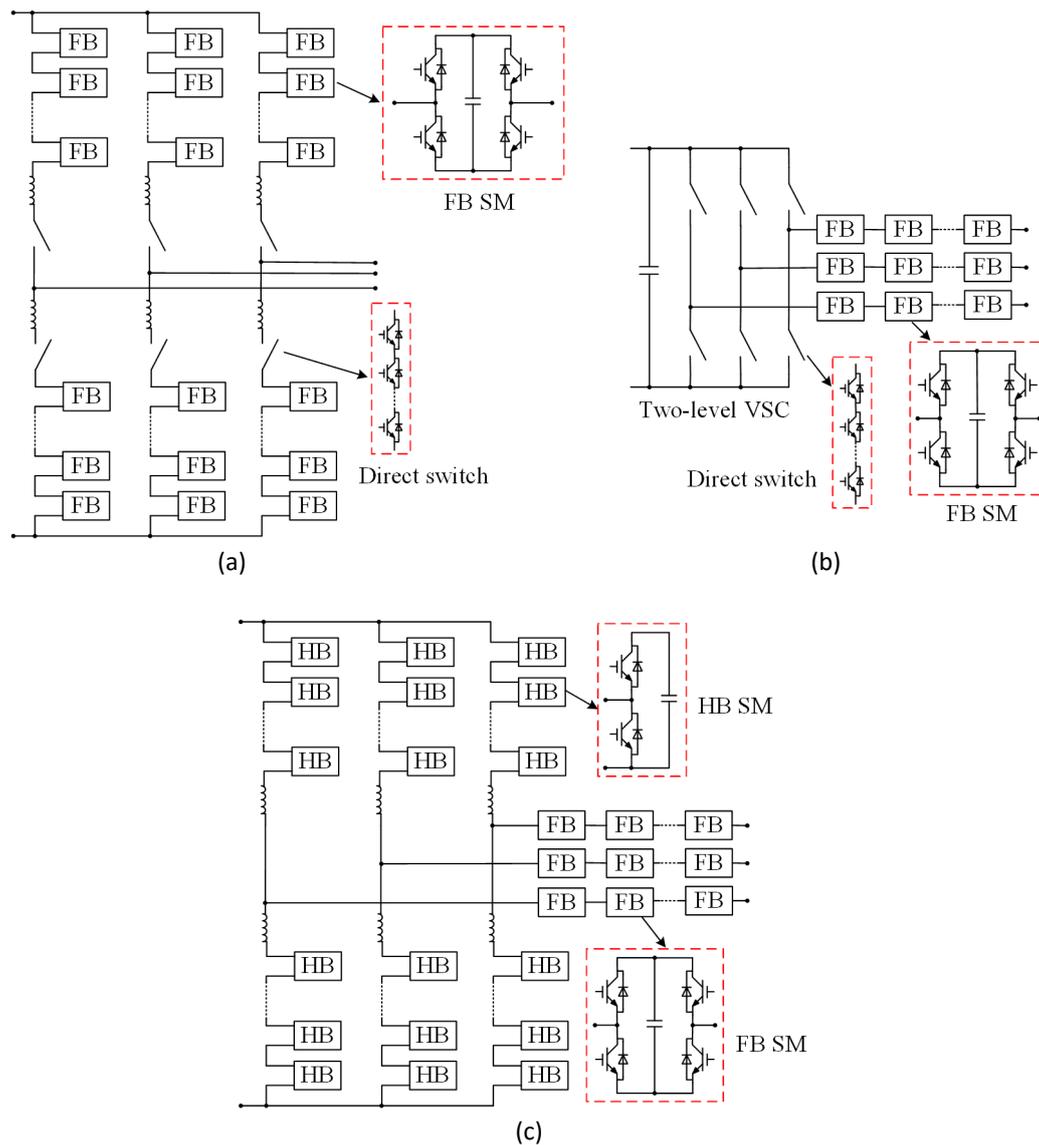
Fig. 5. Alternative topology with DC fault blocking capability: (a) alternate arm converter (AAC) [28-31], (b) hybrid cascaded converter with two-level VSC in the main circuit [5, 37-39], (c) hybrid cascaded converter with MMC in the main circuit [40].

2) Hybrid cascaded converter with two-level VSC in the main circuit (HC-VSC)

References [5, 37-39] present another hybrid multilevel converter configuration which uses the two-level VSC in series with cascaded FB SMs, as illustrated in Fig. 5 (b). Following the blocking of the converter after the DC fault, the cascaded FB SMs provide negative voltages to block the fault current fed from the AC grid to the DC fault. In normal operation, the cascaded FB SMs act as active filter to attenuate the harmonics generated by the two-level VSC and do not contribute to real power transfer. With selective harmonic elimination (SHE) modulation, the switching frequency of the two-level VSC can be very low, e.g. around 150 Hz, yielding reduced switching losses compared to conventional two- and three-level VSCs in HVDC application.

However, the active switches of the two-level VSC still require series connection of IGBTs. A large DC capacitor is required at the DC link of the two-level VSC, which will discharge during a DC fault leading to high DC fault current. In addition, the inrush current from the AC grid during system recovery, when the DC side capacitor is recharged from the AC side to re-establish the DC link

voltage, can potentially be very high and thus additional measures have to be in place to limit this charging current. Furthermore, the use of the two-level converter in the main power stage [5, 37-39, 41, 42] necessitates the cascaded FB SMs (low power stage) to track fast rates of change of voltage (*dv/dt*), which makes synchronization of the two power stages challenging.

3) Hybrid cascaded converter with MMC in the main circuit (HC-MMC)

The proposed hybrid topology in [40] replaces the two-level VSC with the HB-MMC as illustrated in Fig. 5 (c). The large DC link capacitor is eliminated and the large capacitor discharge current after a DC fault is avoided. After the converter is blocked following the fault, the cascaded FB chains can provide reverse blocking voltage. Another advantage of the topology is its soft-restarting capability after DC fault clearance. With the AC-side cascaded FB SMs blocked disconnecting the MMC stage from the AC grid, the HB SMs in the main MMC stage are sequentially connected in the current path after the DC fault isolation to gradually recharge the DC cable using the energy stored in the HB SM capacitors [43]. The soft-restarting capability avoids the large inrush current during rapid change of the DC link voltage after fault clearance.

C. Brief Summaries of Converter Topologies

Although the HB-MMC is incapable blocking DC faults, its losses and semiconductor cost are lower than all other alternatives and is still the preferred topology in today's HVDC projects, e.g. Trans Bay Cable HVDC link (±200 kV, San Francisco, USA), France-Spain HVDC link (underground cable, ±320 kV), Zhangbei 4-terminal HVDC project (±500 kV, near Beijing China) [44, 45].

Due to the negative voltage generating capability, FB-MMCs can not only block DC faults but also provide flexible control, as listed in Table V. FB-MMC has been proposed for HVDC link with overhead lines, e.g. the ULTRANET direct current project (±380 kV, 2 GW, Germany), where DC faults occur relatively frequently compared to its counterpart with cables. FB-MMC stations can quickly extinguish fault current and deionize the arc, and provide fast restart after clearance of temporary faults to minimize power transmission interruption [46]. Mixed SM MMCs offer balanced performances in terms of efficiency, cost, DC fault blocking capability, and control flexibility and are likely to find implementations in HVDC systems in the near future.

For other "hybrid converters", e.g. the AAC and HC-VSC, they do not have the same modular design as the MMC based ones but have their own distinguished features. For example, AAC requires a smaller footprint than that of the HB-MMC, which can be advantageous for applications where space is limited.

IV. DC FAULT PROTECTION

A. DC Fault Detection and Location

In the event of a DC fault on part of a large HVDC network, it is desirable that the fault can be quickly detected and isolated so the healthy part of the DC network can continue operation [47-50].

1) Fault detection and location with local voltage and current measurements

1>. Arm currents

As previously mentioned in Section II B, the converter arm currents flowing through the switching devices increase after a DC fault. To protect the switching devices from being damaged by the large fault current, the arm currents are continuously measured and overcurrent can be used as an indication of faults. If any of the arm currents in the MMC reaches the protection threshold, e.g. 2 p.u., a fault is detected and the converter is immediately blocked [16]. This approach can only detect the fault and protect the converter stations but is incapable of locating the fault.

2>. DC voltage (positive and negative pole voltages)

In HVDC systems, voltage transducers are equipped at each terminal of the MMC station to measure the positive and negative pole-to-ground voltages (v_{Tp} and v_{Tn}, Fig. 1) for used in converter control and over- and under-voltage protection etc. After a DC fault, the DC voltages (i.e. v_{Tp} and v_{Tn}) change significantly, which is an important indicator for detecting the DC fault.

Based on a fault current model, the relationship between the DC link voltage and fault distance is derived to locate the fault without telecommunication [21]. However, the precision of this method is significantly affected by the accuracy of the model. Based on the circuit analysis of the capacitor discharge stage, the fault location approach discussed in [19] is capable of evaluating the fault distance in a meshed DC network. However, it assumes zero fault resistance and with increasing fault resistance, the error of the estimated fault distance increases.

3>. Converter DC terminal current

The DC current of the converter terminal rapidly increases after a DC fault. Thus, once the measured DC current (i_{DC}, Fig. 1) is out of normal range, the DC fault is detected and appropriate protection measures can then be adopted [51].

A differential detection is proposed in [52, 53], where the DC currents are measured at both ends of each cable and the current difference is used to detect and locate the fault. However, telecommunication is required and thus the detection speed and reliability are low, considering communication delays and potential interruptions.

To improve reliability of fault detection, the locally measured DC current is used as the backup for communication failure in [9]. However, the fault location cannot be evaluated accurately and the stations on healthy branches are also likely to be disconnected from the DC network.

4>. Travelling wave fault detection and location

After the DC fault initiation, the fault propagates among the DC grid and can be located by measuring the fault arrival time at different locations. The DC voltage and DC current travelling waves are considered in [54] and [55] respectively. The highest frequency component reaches the relay in the shortest time and can be used to detect the fault. From the local measurements and without fast communication requirement, the wavelet energy is calculated by discrete wavelet transform and a fault is detected once the wavelet energy exceeds the pre-set threshold [54, 55].

5>. Handshaking fault location for multi-terminal systems

A handshaking approach proposed in [56] can identify and isolate the faulty branch in a multi-terminal HVDC system by combinations of DC disconnectors and ACCBs. With the currents flowing into the cables defined as positive, the currents at both ends of the faulty branch (i.e. Cable 1) are positive while at the healthy cables (i.e. Cable 2 and 3) at least one cable current is negative, as illustrated in Fig. 6. In the event of a DC fault, all the ACCBs are opened first to extinguish the fault current. The DC disconnectors whose previously measured fault currents are positive are then opened at zero current, i.e. SW12, SW21, and SW32 in the example in Fig. 6 [58]. The faulty Cable 1 is hence isolated by SW12 and SW21 and the DC voltages of the healthy branch Cable 2 and 3 can be rebuilt by closing the ACCBs. As the DC voltage at Cable 3 restores, SW32 can then be reclosed while SW12 and SW21 remain open as the DC voltage at Cable 1 is low. Power transmission can then restart using Cable 2 and 3.
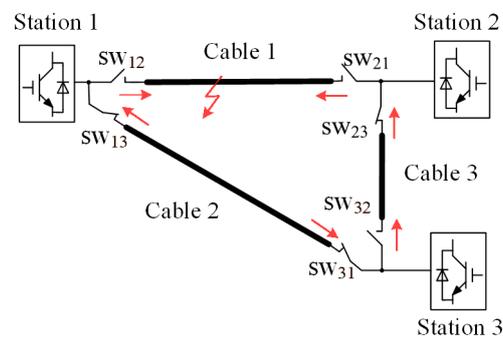

Fig. 6. Handshaking DC fault detection in a three-terminal meshed DC grid with a fault applied at Cable 1 [56].

2) Fault detection and location using the change rate of local measurements

Fault detection based on measured overcurrent leads to slow detection speed especially if the initial DC current is opposite to the fault current due to the considerable time (typically 1-2 ms) required for DC current reversal. For fast DC fault detection, various fault detection methods based on the change rate of local measurements have been proposed [17, 57, 58].

1>. Change rate of DC current

The DC current i_{DC} in Fig. 1 increases after the fault and is governed by

$$\frac{di_{DC}}{dt} = \frac{v_{DC} - v_T}{L_T} = \frac{v_{LT}}{L_T} \tag{1}$$

By considering both the sign and magnitude of the DC current derivative, the fault can be detected and located quickly without using communication. In the presented scheme in [57], a threshold is set to provide faster fault detection and location in a radial multi-terminal HVDC network, yielding low fault current stresses on converter components and circuit breakers.

2>. Change rate of DC voltage

After the fault, the DC voltage v_T (v_{Tp}+ v_{Tn}) after the DC reactor in Fig. 1 drops while the DC terminal voltage v_{DC} still remains at around the rated value in the initial fault stage, due to the large energy stored in the SM capacitors. Thus, from (1), the second derivative of the DC current is given as:

$$\frac{d^2 i_{DC}}{dt^2} = \frac{d}{dt}\left(\frac{v_{DC} - v_T}{L_T}\right) \approx -\frac{d}{dt}\left(\frac{v_T}{L_T}\right) = -\frac{d}{dt}\left(\frac{v_{Tp} - v_{Tn}}{L_T}\right) \tag{2}$$

Equation (2) indicates that the second derivative of the DC current can be simplified by the change rate of the DC voltage. In addition to pole-to-pole DC fault, pole-to-ground fault can also be quickly detected and accurately located by measuring the change rate of both the positive and negative DC voltages ($\frac{dv_{Tp}}{dt}$ and $\frac{dv_{Tn}}{dt}$) [58].

3>. Change rate of the DC reactor voltage

The voltage across the DC reactors (L_T, Fig. 1) is near zero in steady state but increases significantly before the other measureable quantities reacting to the fault. Based on this observation, reference [17] proposes the use of voltages across the DC terminal reactors for fast and accurate DC fault detection in a mesh HVDC grid.

By monitoring the local voltages across the DC reactors, the proposed approach can detect and locate the DC fault much earlier than other methods using the arm currents, DC current or DC voltage. Thus, a fault can be isolated earlier, yielding lower fault current stresses on converters and circuit breakers. In addition, no telecommunication is required. The proposed method is independent with the power flow direction and DC faults with significant short-circuit resistance can still be detected and located accurately.

B. DC Circuit Breaker

Although some converter topologies shown in Section III can block DC faults, these configurations can only prevent overcurrent in the converters and isolating the faulty branch from the healthy network in the HVDC system is still required. Different to DC disconnectors which can only open at zero current, DCCBs are designed to break significant fault current within a very short period (ranging from a few tens microseconds to just over 10 ms). Depending on their configuration, DCCBs are categorized as mechanical, solid-state and hybrid DCCBs.

1) Mechanical DCCBs

As illustrated in Fig. 7 (a), this type of breaker is composed of a mechanical switch in parallel with surge arrestors and resonance circuits. The protection voltage of the surge arrestor is typically 50% higher than the system voltage. During normal operation, the mechanical switch is closed to conduct current. After the fault, the auxiliary switch is turned on to activate the LC resonance circuit to superimpose a resonant current to the fault current to artificially create the current zero-crossing, at which the main mechanical switch can be opened. With the opening of the mechanical switch, the fault current commutates to the parallel surge arrestor, which establishes a counter voltage to reduce the fault current to zero and absorbs the energy stored in the DC line. [59-63].

The losses incurred in mechanical DCCBs are generally low and are negligible compared to the transmitted power. However conventional mechanical DCCBs are slow as the mechanical switch needs relatively long time to open, which typically is around several tens milliseconds. As a result, the converter semiconductors would suffer higher current stress during the response time [64, 65]. However, faster mechanical DCCBs have also been reported [62, 63]. The mechanical DCCBs developed by Mitsubishi Electric Co. Japan can clear DC fault current of 16 kA around 10 ms [63].

ABB also demonstrated that the breaker rated at 80 kV is capable of interrupting fault currents of 10.5 kA within 5 ms [62].
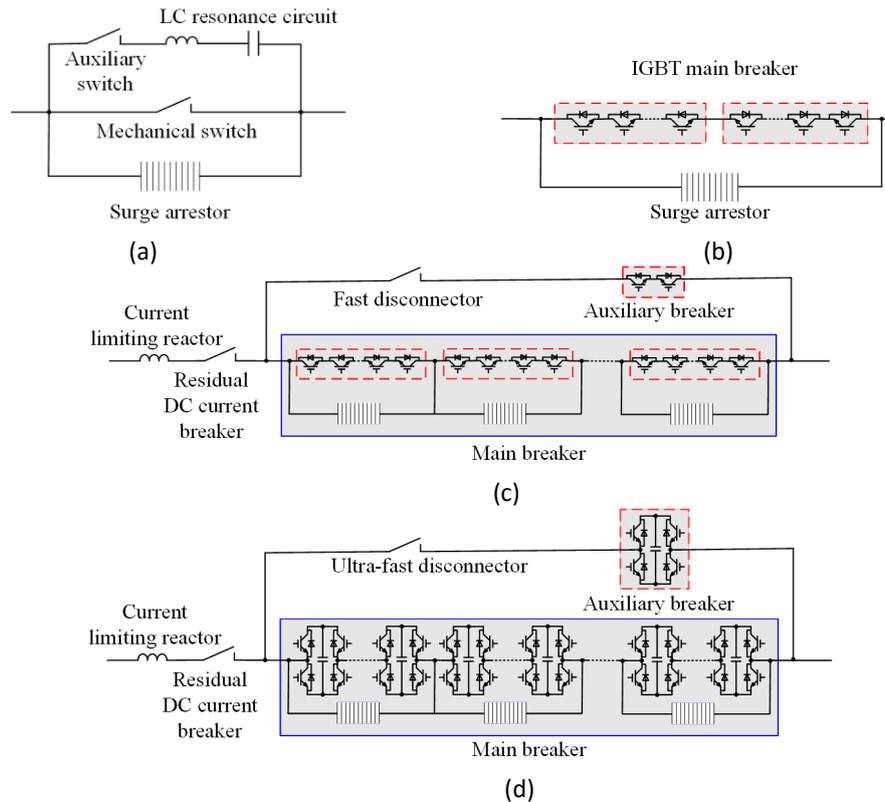

Fig. 7 DCCB circuit: (a) mechanical DCCB [16], (b) solid-state DCCB [66], (c) hybrid DCCB with director switches [59-61], and (d) hybrid DCCB with FB SMs [67].

2) Solid-state DCCBs

The solid-state DCCBs replace the mechanical switch and resonant circuit by series connected semiconductor devices, as illustrated in Fig. 7 (b). The surge arrestors are connected in parallel with the IGBT main breaker to absorb the energy in the DC line and to limit the voltage across the DCCB. Due to the fast action of the IGBTs, such DCCBs can interrupt the fault in less than 1 ms [66]. By connecting solid-state DCCBs at both ends of each cable, the DC fault can be quickly isolated after the fault detection and thus the interruption of remaining service can be avoided [9]. However, this is at the expense of high capital cost and significant on-state operational losses due to the semiconductors in the main current path [8, 9].

3) Hybrid DCCBs

Hybrid DCCBs have been proposed where a mechanical path serves as the main conduction path during normal operation, and a parallel connected main solid-state breaker is used for DC fault isolation, as shown in Fig. 7 (c) [59-61]. On normal operation, all the IGBTs are switched on but the current flows through the fast disconnector and the auxiliary breaker due to the fact that the on-state voltage of the auxiliary circuit is significantly lower than that of the main solid-state breaker (typically in the range of several volts and kV respectively). After fault detection, the auxiliary break quickly opens and the current commutates to the main breaker in the range of a few hundred microseconds, and then the fast disconnector can be opened under zero current. After the opening

of the fast disconnector, the main breaker is deactivated and the fault current then commutates to the surge arrestors, which provide reverse voltage to suppress the fault current. During the opening of the hybrid DCCB, the auxiliary breaker only experiences low voltage stress, i.e. the on-state voltage of the main breaker, and thus its voltage rating is significantly reduced. ABB has completed the laboratory test of such a hybrid DCCB for voltage up to 320 kV and rated current of 2.6 kA [68].

Based on the DCCB circuit in Fig. 7 (c), [67] replaces the series-connected direct switches by FB SMs, as illustrated in Fig. 7 (d), where the SM capacitors are normally bypassed but are inserted in the conduction path after DC faults to provide reverse voltage to block the fault current. The voltage stress of the IGBTs is clamped to the SM capacitor voltage and the voltage sharing issue when series-connecting hundreds of IGBTs is thus avoided. With the SM capacitors bypassed, the energy stored on the SM capacitors is dissipated slowly due to the non-ideal behaviours of devices in practice, such as the capacitor leakage, the equivalent series resistance (ESR), the wiring resistance, and the collector-emitter cut-off current of IGBT. This causes SM voltages to decrease and in order to provide enough voltage to interrupt the fault current, the SM capacitor voltages need to be actively controlled at round the rated value. Alternatively, the SM capacitor voltages are allowed to be zero during normal operation but are quickly charged by the fault current after faults to build up the voltage required for fault current breaking. However, this introduces additional time for the breaker to interrupt the fault current. China State Grid has developed such hybrid DCCBs rated at 200 kV and 2 kA for the Zhoushan 5-terminal MMC-HVDC project (±200 kV, near Shanghai China). They are capable of breaking fault current over 15 kA within 3 ms [67]. This technology is being further developed for use at the ±500kV Zhangbei 4-terminal MMC-HVDC project [69].

Hybrid DCCBs can operate at high speed (within a few ms) and have minimal losses during normal operation. However, they do have relatively large footprint and high capital cost [59-61, 67].

C. Other DC Fault Protection Consideration

1) Inductive fault current limiters (FCLs)

Connecting DC inductors to the station terminals (L_T, Fig. 1) and cable joints can increase the short-circuit impedance, which reduces the rise rates of the arm and DC fault currents, and slows down the fault propagation. This can provide additional time for the DCCBs to isolate the fault without significantly influencing the other healthy parts of the multi-terminal HVDC grid. The fault current experienced by the breakers and the energy absorbed by the surge arrestors are also reduced [16, 53].

However, larger inductors incur increased cost, weight and power losses. Therefore, the trade-off between performance and cost etc. must be carefully considered when selecting the DC inductances. In the Zhoushan 5-terminal MMC-HVDC project, DC inductances of 20 mH were used and connected at the terminals of each station [70-72]. In addition to inductors, nickel wire resistors are used in [73] to limit fault current.

2) Active DC fault current control

As aforementioned in Section II, high voltage is applied across the arm inductors and the DC fault currents rapidly increase after the fault initiation if the DC voltage produced by the converter arms is still controlled at the rated value. To alleviate the fault current, the DC voltage produced by the

converter arms can be lowed by actively regulating the DC component of the arm voltage during Stage I of the DC fault even with HB-MMC. As shown in Fig. 8, a controller is designed to ensure the maximum arm current is not exceeded during a DC fault [16]. As shown, the DC component of the arm currents i_{fault} is obtained by subtracting half of the AC current i_{abc} from the arm current i_{uabc} and is used as the feedback to the controller. The DC component of the arm voltage is reduced by the PID controller from half of the rated DC voltage $\frac{1}{2}V_{DC}$ to $\frac{1}{2}V'_{DC}$ according to the fault current amplitude and thus the fault voltage across the arm inductance is lowered, yielding reduced fault current.
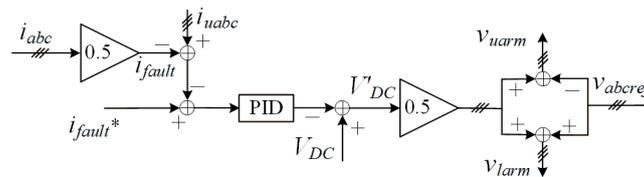

Fig. 8. Active control of DC fault currents for MMCs [16].
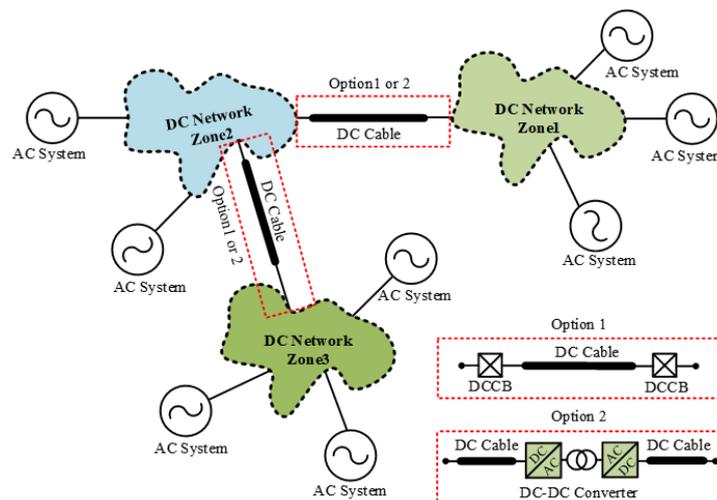
3)   Partitioning DC fault protection

Fig. 9. Partitioned DC fault protection in large DC networks using fast acting DCCBs or DC-DC converter at strategic locations [74].

To rationalize the cost and reliable system operation, network partitioning of a large DC network is proposed in [74-76]. As shown in Fig. 9, fast acting DCCBs or DC-DC converters are only equipped at strategic locations which partition the large DC system into a number of small DC network zones. In case of a fault in one of the DC network zones, the fast acting DCCB (DC-DC converter) is opened (blocked), which acts as a firewall to interrupt the fault propagation, and thus the other healthy DC network zones can remain operational. Within each network zone, relatively slow and cheap protection equipment, e.g. mechanical DCCBs or ACCBs with DC disconnectors, can be used. This ensures the maximum 'loss-of-infeed' for any AC networks connected to the large HVDC system are kept within acceptable limits with reduced investment in protection [74].

V. CONCLUSION

Recent research and development of DC fault protection in MMC based HVDC grid are reviewed in this paper. Due to low impedance of the DC grid, DC faults can result in rapid collapse of DC grid

voltage and fast rise of DC fault current. This can potentially not only cause damage to converter equipment but also lead to the shutdown of the entire DC network. The use of DC fault blocking converters such as those based on FB SMs, mixed SMs etc. enables DC fault ride-through operation of the HVDC station with reduced fault current, but in the expense of additional power devices leading to higher cost and power losses. Regardless of the used converter topologies, the issue of quickly detecting and isolating the DC fault remains a challenge for the development of DC grid. Fast acting DC circuit breakers are currently under development with different configurations and associated operation speeds, costs etc. Significant progresses have been achieved on the hybrid and mechanical types of DC circuit breaker development though further R&D is required before they can become economically and technologically viable. Fast and accurate detection and location of DC faults are also essential for DC fault protection, and various methods are discussed and summarized in this paper. The protection of large DC networks is a challenging task and has to be considered from a whole system approach including converter and DC circuit breaker hardware design, fault detection method, system coordination and control, and the requirement of the connected AC system operation.

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