Compact Mixed Cell Modular Multilevel Converter

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***Abstract*—This paper proposes a new hybrid converter as an alternative to alternate arm converter (AAC) and conventional mixed cell modular multilevel converter (MC-MMC). Although the proposed converter evolves from AAC, it resembles a version of the MC-MMC, where the entire low-voltage rated half-bridge (HB) cells in each arm are replaced by one high-voltage HB cell. Therefore, the proposed converter offers all the tributes of MC-MMC at footprint similar to that of AAC and reduced control complexity as the number of cell capacitor to be control is halved. The practical viability of the proposed converter is confirmed using simulations and experimentations.**

Keywords—Alternate arm converter; mixed cell modular multilevel converter; high-voltage direct current transmission systems; and resiliency to ac and dc faults.

I. INTRODUCTION

In recent years, applications of multilevel converters have increased significantly, particularly, at medium and high voltage distribution and transmission systems [1-4]. This trend started with the development of half and full bridge modular multilevel converters (HB-MMC and FB-MMC), which are seen today as the technology of choice for high-voltage direct current (HVDC) transmission systems [5-9]. Afterward, several multilevel converters were developed in attempt to optimize the power circuits of modular multilevel converters (MMCs) [10-12]. For an example, a MC-MMC has received significant attention in recent years as it permits customized design of the MMC for control flexibility versus semiconductor losses, while retaining many of the attributes of the MMCs such as modularity and internal fault management [8, 10, 13-16]. Beside the commonly used half-bridge and full-bridge (FB) cells, several cell arrangements have been proposed such as the flying capacitor cell, double clamped cell and five-level cells, but most of the MMCs that employ such cells increase complexity of internal fault management without offering new features beyond that offered by the HB-MMC, MC-MMC and FB-MMC [3, 17-20]. In contrast, alternate arm converter (AAC) maintains its attractiveness as it offers dc fault blocking at smaller footprint and lower semiconductor loss compared to MC-MMC and FB-MMC[15, 21]. However, large concentrated dc link capacitor at the input of the AAC for characteristic harmonic filtering represents a major drawback that may impede its use in HVDC transmission systems.

Reference [22, 23] has proposed a thyristor based controlled transition bridge (CTB) converter for ultra-high-voltage direct current (UHVDC) transmission systems, where the full-bridge chain links are employed as forced commutation branches for the thyristors of the six-pulse bridge in the main conduction paths. The proposed arrangement has a potential to reduce the semiconductor losses of the voltage source converter (VSC) to similar level of that of the conventional line commutated converter (LCC). Despite the switching limitations of thyristors employed in the main power stage, the version of the CTB converter in [22, 23] can control active and reactive powers independently; and can operate with zero dc power, while exchanging leading or lagging reactive power as any other VSC, without risk of commutation failure. Nevertheless, the thyristor based CTB converter proposed in [23] requires a number of large ac tuned filters in order to achieve the desired voltage quality for grid operation.

This paper presents a new compact mixed cell modular multilevel converter (CMC-MMC) that evolves from the conventional AAC, and it is developed deliberately with the aim of achieving the control flexibility of the MC-MMC but at footprint similar to that of the AAC (smaller than the MC-MMC). Therefore, the proposed CMC-MMC is well suited for modern point-to-point and HVDC transmission systems and networks, where dc fault blocking and reduced dc voltage operation are advantageous. The rest of the paper is organized as follows: Section II presents a critical review of the conventional AAC as part of the motivation for the proposed CMC-MMC. Detailed description of the fundamentals that underpin the basic operating principle of the proposed CMC-MMC is presented in section 0. Sections IV presents simulation and experimental verifications of the proposed CMC-MMC, where main findings and observations and similarity to conventional MMC are summarized. The main conclusions are drawn in section V.

II. CRITICAL REVIEW OF ALTERNATE ARM CONVERTER

Fig. 1 shows a conventional AAC, with each of its arms comprises of 'N_{FB}' FB cells, a director switch, and an inductor. Its upper and lower arms of the same phase leg conduct the full output phase current alternately, and with each arm conducts for 180° plus overlap period, where both arms of the same phase-leg conduct simultaneously as in the conventional MMC. The overlap period is introduced to allow seamless current commutation from the outgoing arm to the incoming arm and to replenish the cell capacitor voltages of both arms to their desired rated voltages ($½V_{dc}/N_{FB}$). Amongst

several methods suggested for realization of the over-lap period in the AAC, injection of 3rd harmonic into modulation signals is one of the most effective methods that enable satisfactory operation over wide range of modulation indices (see Fig. 2a). The 3rd harmonic injection that maintains constant voltage stresses on the director switches as at the sweet-spot, over the full modulation index linear range is:

$$m^{*}_{abc} = m\sin(\omega t + \gamma_{abc}) + (m - \tfrac{4}{\pi})\sin 3\omega t \qquad (1)$$

where, m is the modulation index. From plots in Fig. 2(a), and output and arm current polarities shown in AAC in Fig. 1, the injection of 3rd harmonic extends the region around the '0' voltage level in the output phase voltage, v_{a0} (which is equivalent to region around the $½V_{dc}$ voltage level in the arm voltage). Fig. 2(a) shows that the effectiveness of the 3rd harmonic injection method diminishes as the modulation index increases, and with the peaks of the modulating signals in Fig. 2(a) remaining fixed at 4/π, independent of 'm'.

Fig. 1 and Fig. 2(b) show that the director switches of the outgoing arms experience significant over-voltages during turn-off (opening) when i_{ao} lags v_{ao}, and this is due to the lack of current path in the outgoing arms. Therefore, the extension of the over-lap period using the 3rd harmonic injection in Fig. 2(a) can avoid or minimize the over-voltage problem in the outgoing arms. For example, when i_{ao} lags v_{ao} by relatively small angle, the overlap period has a potential to allow i_{ao} to change its polarity from negative to positive; thus, finding a path through the freewheeling diode of the director switch of the outgoing arms. When the AAC operates with low power factors lagging (i_{ao} lags v_{ao} by large angles), the over-lap period will only delay the turn-off of the director switches of the outgoing arms to the point where phase currents are relatively small compared to the peak. Thus, with a small arm inductance, the magnitudes and duration of the over-voltage in the outgoing arm could be minimized. When i_{ao} leads v_{ao}, the director switches of the outgoing arms do not experience any overvoltage as the arm currents can find paths through the freewheeling diodes of the director switches. Hence, the current in the outgoing arms would be forced to zero by the capacitors of the inhibited FB cells of the outgoing arms.

Fig. 2c shows voltage waveforms across the FB cells of phase 'a' (v_{FB1} and v_{FB2}), and corresponding arm currents (i_{a1} and i_{a2} scaled by ¼) when the AAC operates at $m=4/\pi$ and 0.95 power factor lagging, and dc link voltage $V_{dc}=300kV$. The voltage waveforms across the director switch and total upper arm shown in Fig. 2d indicate that the director switch of the outgoing arm S_{a1} blocks the peak of the phase voltage ($½mV_{dc}\approx ½\times 4/\pi \times 300kV \approx 191kV$). So, if each IGBT in the string that forms the director switch is rated at $½V_{dc}/N_{FB}$, the number of IGBTs per director switch to enable AAC operation over full modulation index linear range ($0\sim 4/\pi$) is $4/\pi \times N_{FB}$. Notice that the director switches enjoy zero voltage switching during turn-on and turn-off; hence, they incur no switching losses. The AAC director switches must block at least $2/\pi V_{dc}$ should the total voltage across the FB cells of each arm is rated for $½V_{dc}$. Fig. 2(c) and (d) show that the abrupt interruption of the arm currents (i_{a1} and i_{a2}) expose the director switches to fast voltage and current spikes, and their peaks durations depend on the magnitude of the arm inductance. As the effectiveness of the 3rd harmonic injection completely diminishes at $m=4/\pi$ as illustrated earlier in Fig. 2a, Fig. 2(c) shows that the arm currents in the outgoing arms are forced to zero at output voltage zeros (when the total voltage across the full-bridge cells of each arm reaches $½V_{dc}$).

Fig. 3(a) and (b) show v_{FB1} and v_{FB2} and i_{a1} and i_{a2} (scaled by 1/8) when the AAC operates at m=0.9 and 0.5 power factor lagging (power factor angle -60°), with the total voltage across FB cells of each AAC arm remains at $½V_{dc}$. Observe that the injection of the 3rd harmonic into the modulating signals has forced the arm currents to commute several times between outgoing to incoming arms as the director switches of the same phase-leg are gated off and on following modulating signals, without incurring significant switching losses as the voltages across the director switches are practically zero. Fig. 3 (a) and (b) point out that the outgoing arms continue to experience over-voltages due to lack of current path (but the magnitudes of these over-voltages remain lower than the rated blocking voltage of a single director switch).

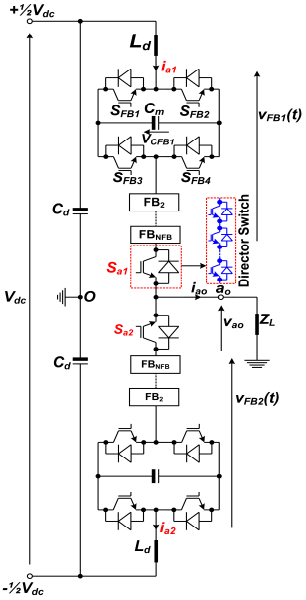
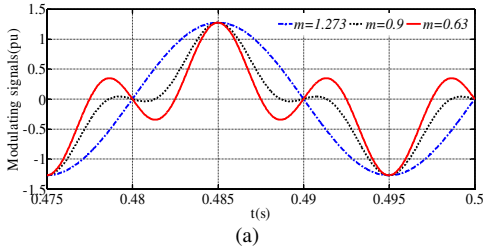
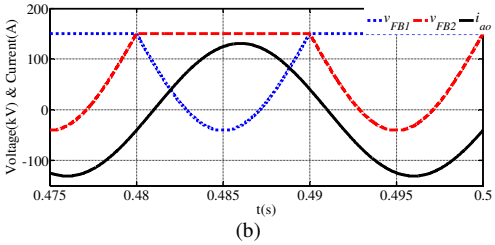


Fig. 1: Conventional AAC



(a)



(b)

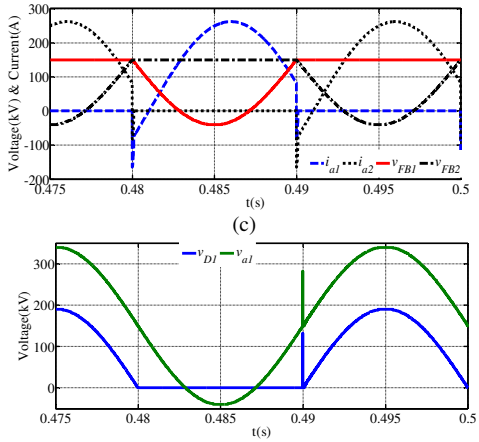


Fig. 2: Waveforms illustrate AAC operation when it supplies a passive load equivalent to 300MVA and 0.95 power factor lagging, 4/π modulation index and 300kV dc link voltage

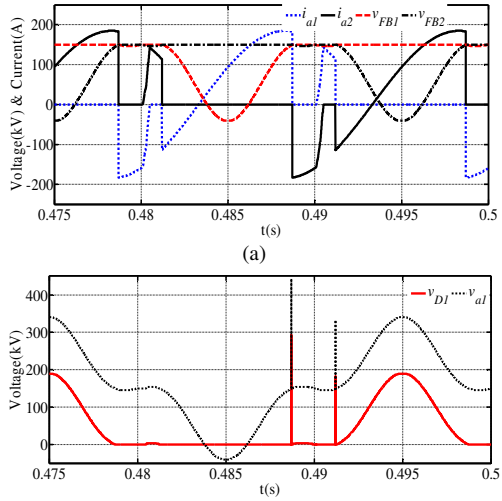


Fig. 3: Waveforms illustrate AAC operation when it supplies a passive load equivalent to 300MVA and 0.5 power factor lagging, 0.9 modulation index, 300kV dc link voltage and with total voltage of FB cells of each arm is $½V_{dc}≈150kV$

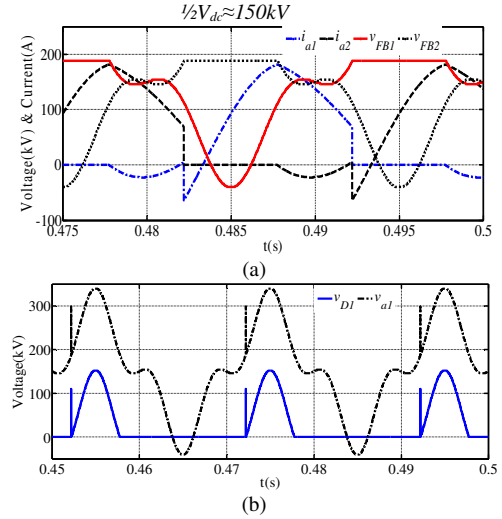


Fig. 4: Waveforms illustrate AAC operation when it supplies a passive load equivalent to 300MVA and 0.5 power factor lagging, 0.9 modulation index, 300kV dc link voltage and full-bridge cells of each arm are rated to block $1.25×½V_{dc}≈187.5kV$

To further minimize the overvoltage problem in the outgoing arms, the number of FB cells in each AAC arm could be increased to block more than $½V_{dc}$ in order to allow typical MMC operation over a limited number of voltage levels above and below '0' voltage level in the output voltage v_{ao} (simultaneous conduction of upper and lower arms of the same phase-leg). Fig. 4(a) and (b) show v_{FB1} and v_{FB2} and i_{a1} and i_{a2} (scaled by 1/8) when the AAC operates at m=0.9 and 0.5 power factor lagging, but this time the total voltage across the FB cells of each arm is increased to $1.25×½V_{dc}$. Observe that the use of additional FB cells in the AAC arms allows better exploitation of the extended regions around zero voltage level (where AAC can operate as MMC with simultaneous conduction of both arms of the same phase-leg) in order to avoid or minimize the over-voltages in the outgoing arms. With additional FB cells in each AAC arm, the director switch rated voltage can be reduced to $½V_{dc}×(4/π-k+1)$, where $k=N_{FB}/N_{FB0}$, and N_{FB0} represents the number of cells corresponding to the total voltage across FB cells of each arm of $½V_{dc}$.

In summary, the above discussions show that the conventional AAC requires large number of FB cells to operate correctly over full power factor and modulation index range. Its large concentrated dc link capacitance, which is needed for filtering of the characteristic harmonics from the dc link current dc fault level.

III. COMPACT MIXED CELL MODULAR CONVERTER

Fig. 5 shows the proposed CMC-MMC, which is developed by replacing the director switch in each AAC arm by equivalent high-voltage half-bridge (HV-HB) cell. The switching devices and capacitor of the HV-HB cell is rated at $½V_{dc}$. Similarly, the combined rated voltage of the FB cells per arm is $½V_{dc}$. The use of high-voltage HV-HB cell instead of the director switch allows the CMC-MMC to be operated as an AAC or MMC, without any difficulties of the conventional AAC discussed in section II. However, this paper abandons the AAC operation in favour of typical MMC operation due to increased utilization of current carrying capability of the switching devices. Therefore, the presented CMC-MMC adheres to the same operating principle of the MMC, with voltages across phase 'a' upper and lower arms could be approximated by:

$$v_{a1}(t) = \tfrac{1}{2}V_{cap}(1 - m\sin\omega t) \quad (2)$$

$$v_{a2}(t) = \tfrac{1}{2}V_{cap}(1 + m\sin\omega t) \quad (3)$$

where V_{cap} represents the average capacitor voltage sum per phase-leg. Consider phase 'a' as an example, switching of the 'N_{FB}' FB cells and the HV-HB cell of the upper and lower arms must be coordinated in order to correct synthesis of the arm voltages described in (2) and (3). Therefore, phase 'a' upper and lower arm voltages can be expressed as:

$$v_{ahb1} + v_{afb1} = \tfrac{1}{2}V_{cap}(1 - m\sin\omega t) \quad (4)$$

$$v_{ahb2} + v_{afb2} = \tfrac{1}{2}V_{cap}(1 + m\sin\omega t) \quad (5)$$

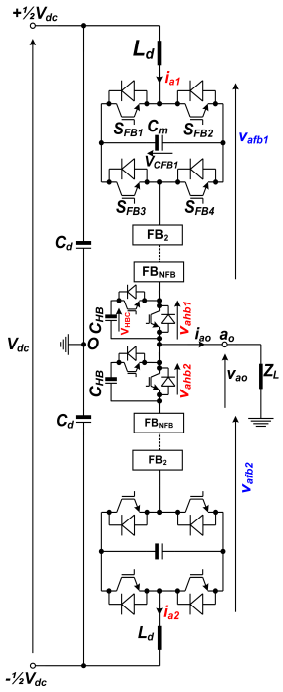


Fig. 5: The proposed compact mixed cell modular converter

When V_{cap} and voltage across capacitor of the HB cell of each arm are more likely to be regulated at V_{dc} and ½V_{dc}, the FB cells of the upper and lower arms must be controlled to synthesize the following voltages:

For $0 \le \omega t \le \pi$

$$v_{afb1}(t) \approx v_{a1}(t) - v_{ahb1}(t) \approx \begin{cases} -\frac{1}{2} m V_{dc} \sin \omega t & \text{when } v_{ahb1}(t) = \frac{1}{2} V_{dc} \\ \frac{1}{2} V_{dc}(1 - m \sin \omega t) & \text{when } v_{ahb1}(t) = 0 \end{cases} \quad (6)$$

$$v_{afb2} = v_{a2}(t) - v_{ahb2} = ½ m V_{dc} \sin \omega t \quad (7)$$

For $\pi \le \omega t \le 2\pi$

$$v_{afb1} = v_{a1}(t) - v_{ahb1} = -½ m V_{dc} \sin \omega t \quad (8)$$

$$v_{afb2}(t) \approx v_{a2}(t) - v_{ahb2}(t) \approx \begin{cases} \frac{1}{2} m V_{dc} \sin \omega t & \text{when } v_{ahb2}(t) = \frac{1}{2} V_{dc} \\ \frac{1}{2} V_{dc}(1 + m \sin \omega t) & \text{when } v_{ahb2}(t) = 0 \end{cases} \quad (9)$$

The two distinct switch combinations for synthesis of the arm voltages described in (6) and (9) could be exploited to minimize the deviation of the HV-HB cell capacitor voltage of each arm from ½V_{dc}, whilst the Marquardt sorting based capacitor voltage balancing can be used to ensure the inter-cell balancing of the FB cells. As in conventional MMC, the upper and lower arm and output currents of the CMC-MMC are:

$$i_{a1}(t) = I_d + ½ i_{a0}(t) + i_h(t) \quad (10)$$

$$i_{a2}(t) = I_d - ½ i_{a0}(t) + i_h(t) \quad (11)$$

$$i_{ao}(t) = i_{a1}(t) - i_{a2}(t) \quad (12)$$

where, $I_d \approx ⅓ I_{dc}$ represents the dc component of the arm current, $i_{ao}(t)$ is the output current, and $i_h(t)$ is the circulating current.

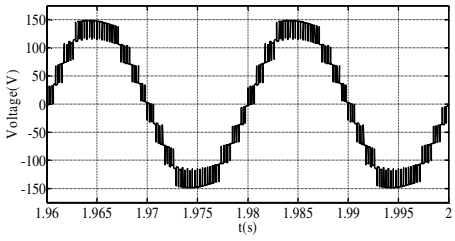
IV. Simulations and Experimentations

A. Simulations

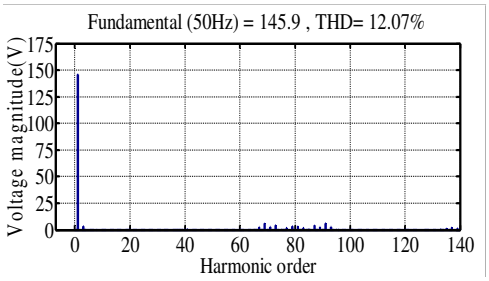
This section presents basic simulations that substantiate the theoretical discussions of the CMC-MMC presented in section 0, considering the steady-state operation of CMC-MMC when it is supplying a passive load. The CMC-MMC simulation parameters in this illustration are summarized as follows: V_{dc}=300V; unity modulation index; level shifted carriers with 2kHz switching frequency; arm inductance, L_d=5mH; N_{FB}=2; HV-HB and FB cell capacitances are C_{HB}=1mF and C_{FB}=2mF; and passive load resistance and inductance are 10Ω and 15mH.

Fig. 6(a) and (b) show a pre-filter phase voltage 'v_{ao}' the CMC-MMC presents to the passive load connected to its ac side and its spectrum. Observe that the CMC-MMC with only one HV-HB and two FB cells, generates nine voltage levels per phase (generically, CMC-MMC with 'N_{FB}' FB cells per arm generates '$4N_{FB}+1$' voltage levels per phase). See that the total harmonic distortion (THD) for the simulated case is 12%, with the spectrum of phase voltage in Fig. 6(b) indicates that no harmonics exist in the baseband, no switching frequency component, and only sideband harmonics are present around the 1st and 2nd switching frequency components, which are easily attenuated with small ac filters. The traces for the output phase and upper and lower arm currents when circulating currents are not suppressed are shown in Fig. 6(c). Additional plots when modulation index is 0.9 and circulating currents are suppressed are shown in Fig. 7. The plots for the output phase voltage and current, upper and lower arm currents, half and full bridge capacitor voltages and common and differential mode capacitor voltage sums in Fig. 7(a) to (d) plus that presented in Fig. 6 confirm that the proposed CMC-MMC adheres to the same mathematical relationships that govern the operation of conventional MMC as stated earlier and equations (10) to (12). The main observations are summarized as:

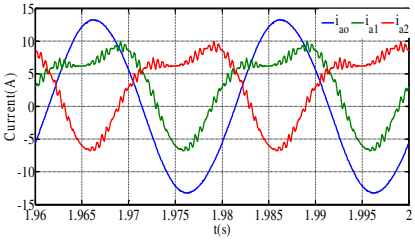
1) Each arm current inherently comprises of dc current (I_d), fundamental current (½i_{ao}) and circulating current i_h (which is dominantly 2nd harmonic). So, the circulating current must be suppressed as in conventional MMC.
2) The inherent 2nd harmonic exist in the common-mode capacitor voltage sum (V_{com}) is the main driver for the circulating current in CMC-MMC arm as in conventional MMC, see Fig. 7(c).
3) The differential-mode capacitor voltage sum. (V_{dif}) is dominantly fundamental current as in conventional MMC, see Fig. 7(c)
4) The CMC-MMC with N_{FB}=N_c and one HV-HB cell per arm generates the same number voltage levels per phase as MC-MMC with N_{FB}=N_{HB}=N_c. This means both the quality of its output voltage and *dv/dt* remain the same as conventional MC-MMC.



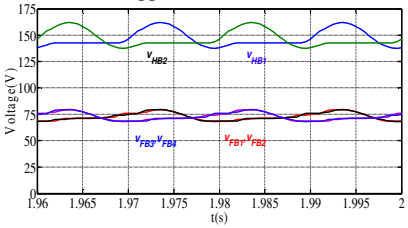
a) Pre-filter phase '*a*' output voltage 'v_{ao}'



b) Spectrum of phase voltage 'v_{ao}'

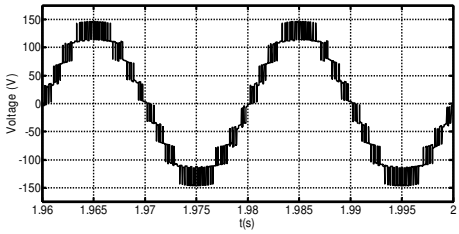


c) Phase '*a*' output current superimposed on its corresponding upper and lower arm currents

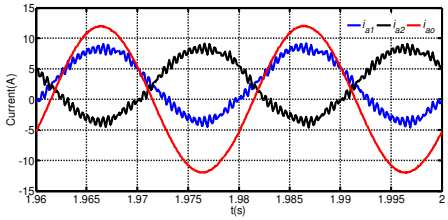


d) Capacitor voltages of the full and half bridge cells of phase '*a*'

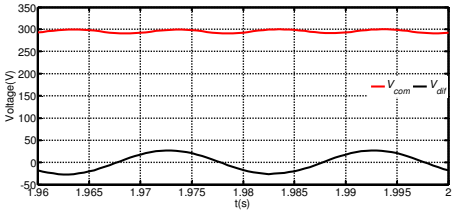
Fig. 6: Simulation waveforms that illustrate the basic behaviour of the CMC-MMC (m=1 and without circulating current controller)



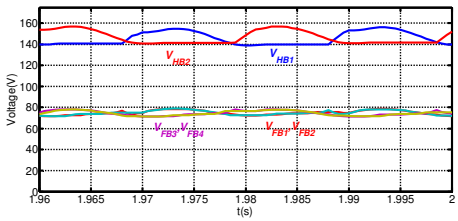
a) Phase '*a*' voltage 'v_{ao}'



(b) Phase '*a*' output current 'i_{ao}' superimposed on its corresponding upper and lower arm currents, i_{a1} and i_{a2}



(c) Common and differential capacitor voltage sums



(d) Capacitor voltage of the full and half bridge cells

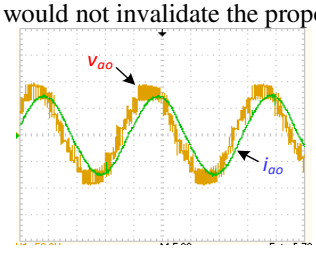
Fig. 7: Simulation waveforms that illustrate the basic behaviour of the CMC-MMC when m=0.9 and with circulating current controller

B. *Experimental validation*

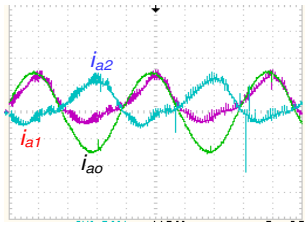
To substantiate the discussions and simulation results presented in sections 0 and IV-A, experimental results obtained from a prototype of the CMC-MMC are presented in Fig. 8. Detailed parameters of the experimental test rig as follows: 220V dc link, level shifted carrier with 2kHz carrier frequency, 0.95 modulation index and passive load of 10Ω and 15.5mH.

Fig. 8(a) shows the prototype of the proposed CMC-MMC with one HB cell and two FB cells per am presents high quality output voltage (v_{ao}) across the passive load, and sinusoidal load current (i_{ao}). Fig. 8(b) displays the experimental waveforms for the upper and lower arm currents of the CMC-MMC overlaid on the output phase current. These waveforms confirm the adherence of the CMC-MMC to the same fundamentals that underpin the operation of conventional MMC as stated earlier. Fig. 8 (c) and (d) show the HV-HB and FB capacitor voltages are tightly controlled around the desired set-points of $½V_{dc}$ (110V) and $¼V_{dc}$ (55V) respectively. The experimental waveforms presented in Fig. 8 show that the use of HB cell rated for $½V_{dc}$ in each arm of the CMC-MMC does not affect commutation between the cells of the same arm nor between the upper and lower arms of the same phase leg.

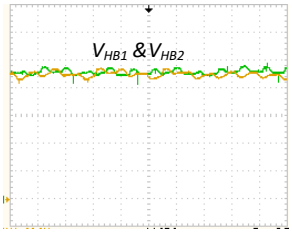
In summary, these results confirm that the replacement of large number of low-voltage rated HB cells as in conventional MC-MMC by one HV-HB cell in each arm of the proposed CMC-MMC does not increase the *dv/dt* on the ac side load nor in the arm. It is worth emphasizing that the practical realization of series connected IGBT up to 400kV has a precedence in [24]; therefore, the use of HV-HB cell which rated for $½V_{dc}$ would not invalidate the proposed CMC-MMC.



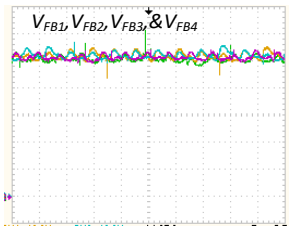
(a)



(b)



(c)



(d)

Fig. 8: Experimental waveforms that confirm the validity of the proposed CMC-MMC, with (a) phase voltage 'v_{ao}' superimposed on phase current 'i_{ao}' (5ms/DIV, 50V/DIV), (b) output phase current 'i_{ao}' superimposed on the upper and lower arm currents 'i_{a1} and i_{a2}' (5ms/div, 5A/div), (c) capacitor voltages of the half-bridge cells (25ms/div, 20V/div), and (d) capacitor voltages of the full-bridge cells (25ms/div, 10V/div)

V. CONCLUSIONS

This paper has presented a comprehensive review of the state-of-art multilevel voltage source converters, with particular emphasis on topologies, with the aim of finding the best design trade-off for HVDC converters. The outcome of this review has provided a critical motivation for the development of CMC-MMC, which has been explored and extensively discussed in this paper. The presented simulation and experimental results show that the proposed CMC-MMC has potential to offer the best design compromise for HVDC converters in terms of control flexibility, footprint and weight and resiliency to ac and dc network faults.

VI. .REFERENCES

[1] G. P. Adam, I. A. Gowaid, S. J. Finney, D. Holliday, and B. W. Williams, "Review of dc-dc converters for multi-terminal HVDC transmission networks," *IET Power Electronics,* vol. 9, pp. 281-296, 2016.

[2] O. E. Oni, I. E. Davidson, and K. N. I. Mbangula, "A review of LCC-HVDC and VSC-HVDC technologies and applications," in *2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC)*, 2016, pp. 1-7.

[3] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 4-17, 2015.

[4] J. Glasdam, J. Hjerrild, L. H. Kocewiak, and C. L. Bak, "Review on multi-level voltage source converter based HVDC technologies for grid connection of large offshore wind farms," in *Power System Technology (POWERCON), 2012 IEEE International Conference on*, 2012, pp. 1-6.

[5] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable Modular Multilevel Converters for HVDC-transmission," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 174-179.

[6] A. Lesnicar, and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, 2003, p. 6 pp. Vol.3.

[7] C. Oates, and C. Davidson, "A comparison of two methods of estimating losses in the Modular Multi-Level Converter," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, 2011, pp. 1-10.

[8] C. C. Davidson, D. R. Trainer, C. D. M. Oates, R. W. Crookes, N. M. Macleod, and D. R. Critchley, "A new hybrid voltage-sourced converter for HVDC power transmission," presented at the Cigre, Paris, 2010.

[9] C. Oates, "A methodology for developing Chainlink converters," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, 2009, pp. 1-10.

[10] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and Operation of a Hybrid Modular Multilevel Converter," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 1137-1146, 2015.

[11] W. Kui, L. Yongdong, Z. Zedong, and X. Lie, "Voltage Balancing and Fluctuation-Suppression Methods of Floating Capacitors in a New Modular Multilevel Converter," *Industrial Electronics, IEEE Transactions on,* vol. 60, pp. 1943-1954, 2013.

[12] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," in *Transmission and Distribution Conference and Exposition (T&D), 2012 IEEE PES*, 2012, pp. 1-1.

[13] C. Oates, "Modular Multilevel Converter Design for VSC HVDC Applications," *Emerging and Selected Topics in Power Electronics, IEEE Journal of,* vol. PP, pp. 1-1, 2014.

[14] C. Oates, K. Dyke, and D. Trainer, "The augmented modular multilevel converter," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014, pp. 1-10.

[15] C. Oates, K. Dyke, and D. Trainer, "The use of trapezoid waveforms within converters for HVDC," in *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, 2014, pp. 1-10.

[16] G. P. Adam, S. J. Finney, B. W. Williams, D. R. Trainer, C. D. M. Oates, and D. R. Critchley, "Network fault tolerant voltage-source-converters for high-voltage applications," in *AC and DC Power Transmission, 2010. ACDC. 9th IET International Conference on*, 2010, pp. 1-5.

[17] A. Nami, L. Jiaqi, F. Dijkhuizen, and G. D. Demetriades, "Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities," *Power Electronics, IEEE Transactions on,* vol. 30, pp. 18-36, 2015.

[18] G. P. Adam, I. Abdelsalam, J. E. Fletcher, G. Burt, D. Holliday, and S. J. Finney, "New Efficient Sub-module for Modular Multilevel Converter for Multi-terminal HVDC Networks," *IEEE Transactions on Power Electronics,* vol. PP, pp. 1-1, 2016.

[19] G. P. Adam and I. E. Davidson, "Robust and Generic Control of Full-Bridge Modular Multilevel Converter High-Voltage DC Transmission Systems," *IEEE Transactions on Power Delivery,* vol. 30, pp. 2468-2476, 2015.

[20] G. P. Adam, S. J. Finney, and B. W. Williams, "Enhanced control strategy of full-bridge modular multilevel converter," in *2015 International Conference on Renewable Energy Research and Applications (ICRERA)*, 2015, pp. 1432-1436.

[21] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer†, D. R. Critchley†, and R. W. Crookes†, "A New Hybrid Multi-Level Voltage-Source Converter with DC Fault Blocking Capability," in *IET ACDC2010*, London,UK, 2010.

[22] P. Li, S. J. Finney, and D. Holliday, "Thyristor based modular multilevel converter with active full-bridge chain-link for forced commutation," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2016, pp. 1-6.

[23] P. Li, G. P. Adam, S. J. Finney, and D. Holliday, "Operation Analysis of Thyristor Based Front-to-Front Active-Forced-Commutated Bridge DC Transformer in LCC and VSC Hybrid HVDC Networks," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. PP, pp. 1-1, 2017.

[24] J. Egan, P. O. Rourke, R. Sellick, P. Tomlinson, B. Johnson, and S. Svensson, "Overview of the 500MW EirGrid East-West Interconnector, considering System Design and execution-phase issues," in *Power Engineering Conference (UPEC), 2013 48th International Universities'*, 2013, pp. 1-6.