Regions of Electrical Stress in High Voltage Capacitor Units

Calum J. Mackinnon[1], Brian G. Stewart[1]

1. Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, Scotland

Abstract – As electrical systems develop, and power electronic converter interfaces proliferate, greater reliance is placed on the capacitor units which comprise them. For such applications, resilience to electrical stresses is essential to capacitor unit design, as electrical field stresses can degrade insulation and cultivate incipient faults. Left unchecked, insulation can breakdown and cause an associated reduction in capacitance, an increased reactance, and subsequently greater electric field stresses and susceptibility to further 'cascading' failures. COMSOL Multiphysics'® AC/DC module is used in this study to emulate electric field stresses throughout a simplified capacitor unit. Regions of electrical field stress are highlighted using an electrostatics boundary condition so that: their impact and implications for fault progression can be considered for engineering design; and to inform maintenance activities of where degradation is anticipated. While this study uses a simplistic capacitor model of homogenous dielectric, few winding turns, and omits noise inherent to real applications, it could offer limited insight into physical influences within enclosed assets which are presently becoming increasingly pervasive in electrical infrastructure. Configurability is also discussed as a means to enable study of alternative designs.

Keywords: Capacitors, Electrical Power Systems

I. Introduction

Modern electrical power networks include an increasing prevalence of power electronic interfaces, which allow diversity in supply and demand, control over power flows, and asynchronous connections needed for renewable resources and interconnection.

High voltage capacitor banks offer a dual role for large scale high-voltage direct current (HVDC) interconnection converter stations: they form part of tuned filtering arrangements; and provide reactive power support necessary to support an interface between a conventional HVDC converter station and the wider AC network it connects to.

Despite an increasing prevalence in electrical power infrastructure due to a growth of HVDC and other power electronic applications (such as reactive power compensation, for instance), and despite therefore becoming correspondingly more critical to network reliability, at present fault location and monitoring for high voltage capacitors has received "little" attention in academic literature [1].

This paper considers the influence of electrical field stresses on dielectrics in high voltage capacitor units. A high-voltage discrete foil capacitor with interleaved winding design is modelled, to approximate those which might be used at HVDC converter stations. It aims to investigate regions of electrical field stress within such capacitor units, primarily to raise awareness of these areas of heightened stress to inform capacitor module design.

Section II offers brief technical background to capacitor units for power system applications, before a simulation setup overview is provided in Section III. Section IV discusses the simulation studies conducted in this study, of which some results are presented in Section V. In turn, these results are discussed in Section VI, with Section VII offering commentary on the methodology used, before conclusions are finally drawn in Section VIII.

II. Background

Capacitive element windings are made with layers of dielectric, which are rolled together with metallic terminals, to maximise the surface area between them. Dielectric can be Kraft paper impregnated with mineral oil, but in modern designs polypropylene layers are typically used. Multiple dielectric layers can be used to limit the effects of manufacturing defects and improve reliability.

Windings can have two or more terminals, where each end has one terminal available for a connection to be made, and where intermediate terminals are physically unconnected but have interleaving cross-sectional areas to give rise to series-connected capacitances, as in Figure 1.

As also shown in Figure 1, each end of a winding has one terminal extended slightly beyond the dielectric layer and a margin of dielectric protects the other terminal. This is an extended-foil design, which allows "schooping" to make a connection where an extended terminal is soldered at one end, in the knowledge that the next terminal is protected from the solder by the dielectric margin. Otherwise, connections can also be made with foil tabs soldered to individual terminal layers and jump leads can be used to connect winding groups. By these means: element windings can be connected in groups; these groups can be connected as a set; and in turn, the set of winding groups can connect to the module terminal bushings at one end of the unit housing. If a design has an uneven number of windings, a draw lead can connect a bushing to the far end of a unit.

Windings, groups, and capacitor modules can connect in series or parallel, each so that a bank can be respectively configured to accommodate high voltages or to support reactive power.

Terminals are typically aluminium foils for discrete-foil designs which are considered more efficient than a reliable alternative: metallised-film capacitor designs, in which dielectric layers are sprayed with metallised vapor to create terminals which vaporise in the event of a dielectric breakdown, to thereby protect the vicinity of the dielectric fault afterwards. Discrete foil designs are more common in high-capacity converter stations due to their efficiency.

Discrete foil units can include fuses: externally fused; internally fused; and fuseless designs allow trade-offs between resilience to faults and efficiency during normal operation. Discharge resistors are used to safely dissipate charge after a disconnection.

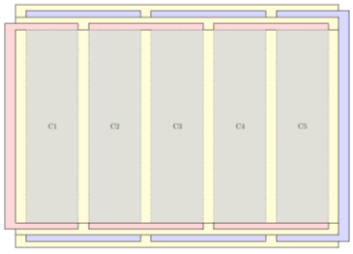

Figure 1: A set of elements as one winding

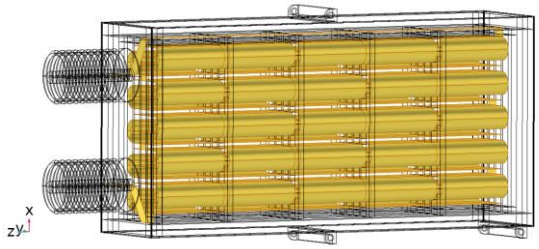

Figure 2: A capacitor model geometry

Units are housed with a metal enclosure and sit on a rack in a capacitor bank. Since racks are at voltage, so too is the capacitor housing. A limited number of capacitor units are therefore used on each rack, to limit potential differences between housing and the capacitive element windings, and each capacitor unit is typically filled with dielectric fluid to insulate the housing from the elements it contains.

By their role and position within converter stations, capacitor banks are subject to impulses from switching, converter operation, and any associated harmonics. Limited data are publically available to describe capacitor bank operation or longevity in such settings, possibly since the uptake of power electronic technologies in electrical power infrastructure is a recent development in the context of established alternating current infrastructure. As such, model-based approaches are paramount in developing an understanding of where and how electrical stresses can arise in capacitor units, which can degrade insulation and cultivate incipient faults.

III. Experimental Setup

This study uses a discrete-foil, high-voltage capacitor model (Figure 2) developed in COMSOL Multiphysics®. It has five interleaved windings, each of five series capacitances, aligned along the Z-axis of the model geometry. These windings are connected in series at alternate ends of the module, with a draw lead to make the low-voltage connection along the length of the module to the bushing, where the draw lead, its associated foil terminal, and the housing are all assumed to be at ground potential.

The model geometry can best be described in layers: a central volume defines the space in which parallel, flat foil faces are separated by layers of dielectric intended to form the bulk of the capacitance; around which a second layer creates space in which foils fold and allows space necessary to scale a mesh; encompassing this layer is one for dielectric fluid to insulate capacitive elements from an outer housing; and a final narrow layer is defined to be that housing.

Lastly, additional features such as rack mounts, bushings, and connecting leads are included to finalise the geometry and to provide the option for detailed effects (of a draw lead, for example) to be explored when boundary conditions are applied.

This layered approach is important in cultivating an efficient mesh, particularly to allow parameters to be used to define a design with many foils, spaced narrowly, toward more representative asset models.

Parameters are used throughout, to define the space allocated to each layer according to each axis, where symmetry (equal distance on each side) is assumed. Global parameters used to establish a geometry allow that geometry to be easily altered, improve geometry sequence readability, and support for conditional nodes in COMSOL geometry sequences allows users to set parameters even to change the nature of the model simulated from one model file. Model parameters for the file used in this study, for instance, specify: an orientation of foils and their folds according to each axis; a number of windings; a number of turns by which each winding element is folded; and an overall size and shape of the unit.

While windings and foil turns are defined to occupy the entire volume of a capacitor module, domains are specified to create perpendicular divisions. These divisions mean definitions can be selectively applied to each winding to specify each as either: a single capacitive element; or as an interleaved series-connected group of elements spaced with dielectric margins, as illustrated in Figure 1 [2]. Foils are two-dimensional boundaries, and dielectric layers are omitted from the geometry for simplicity so can be assumed to occupy the remaining volume.

An odd number of windings necessitates use of a draw lead to connect all windings in series and make the 'ground' bushing connection [3], included to demonstrate its role in shaping electrical stresses within a unit, albeit with two-dimensional foil boundaries to maintain a simplistic geometry.

Although modern unit designs use polypropylene films, the dielectric is set as transformer oil of relative permittivity 3.9 to approximate mineral oil impregnated Kraft paper, which constitutes a more traditional high voltage capacitor design. Housing is defined as steel, foils as aluminium, and a user-specified porcelain is established for the bushings.

IV. Simulation

A two-step process is followed: firstly, an electrical circuit interface is configured and coupled with one for electric currents to ascertain the distribution of voltages across foils within the unit modelled. Secondly, these voltages are again specified in an electrostatics interface to study electric field stress. With this process, the effects of a ground connected draw lead and application of a 10 kV source are investigated using a steady-state study.

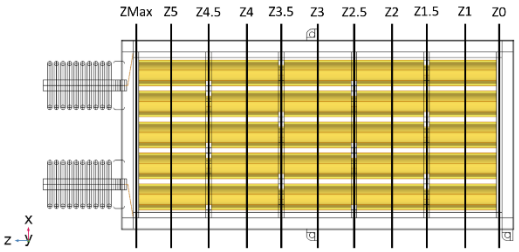

Figure 3: Index for cut planes

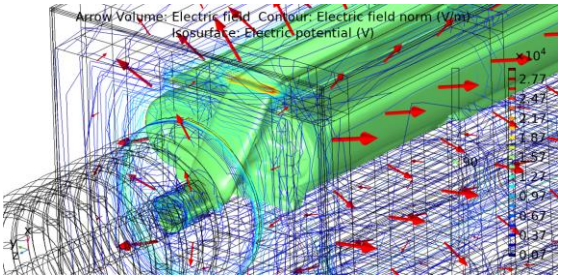

Figure 4: Visualisation techniques in COMSOL

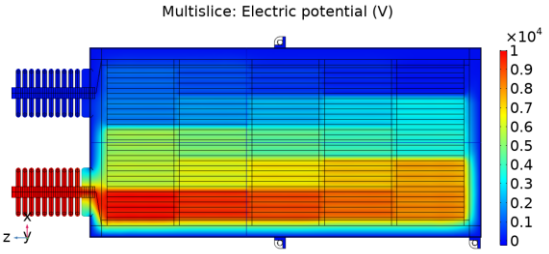

Figure 5: Voltage distributed in the capacitor model

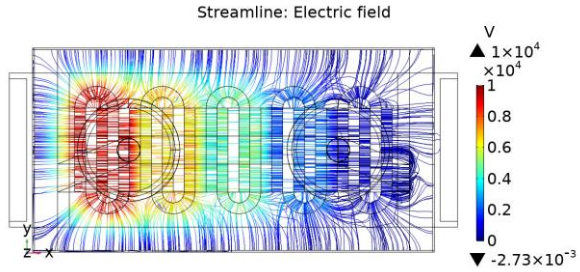

Figure 6: Cross-section of electric field streamlines

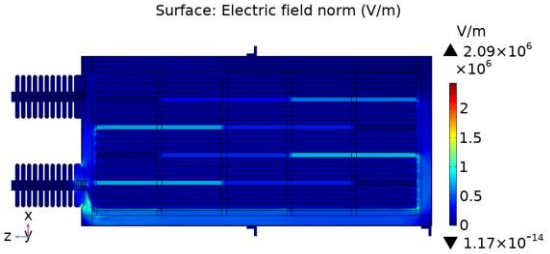

Figure 7: Cut plane through module centre

V. Results

Figure 4 illustrates visualisation options available in COMSOL by showing electrical effects within the model. It shows an isosurface set to 90% of the maximum voltage which encapsulates the high voltage winding and draw lead, and an arrow volume and contour lines to reveal electric field direction and strength. Figure 6 illustrates another visualisation technique available in COMSOL, where streamlines are used to show the electric field. With streamlines coloured according to voltage, it shows how a draw lead distorts the field, some fringing effects between adjacent windings, and the potential for unintended parasitic (stray) effects to arise between adjacent foils and a module housing.

Figure 3 indicates the placement of cut planes along the Z axis of the module geometry. Figure 5 shows the distribution of voltage in the capacitor unit graphically, where values are presented in Table 1 (in an order to match the orientation of Figure 5), and Figure 7 highlights how these voltages incite regions of electric field stress within the model due to its series-connected interleaved winding design.

Choice cut plane diagrams are included in Figures 10, 11, and 12, to show where electric field stresses arise throughout the model. Colour legends are common to all figures aside the latter two diagrams of Figure 10, which respectively show field stress on the inner and outer sides of a draw lead, while the topmost diagram in Figure 10 shows field strength between windings 4 and 5. Figure 11 shows electric field stresses between windings and the housing on an XZ plane, where heightened stress can be seen to accord with winding voltages. Figure 12 comprises XY cut plane diagrams positioned at Z2, Z2.5, and at ZMax as indexed by Figure 3, which respectively reveal electrical field stresses bisecting foil overlaps, overlaps with dielectric margins, and the bushing end, of each of the set of five capacitive windings.

Cut lines aligned with the X axis are specified at each point on the Z axis identified by Figure 3, and at three Y axis positions: the centre (YMid); and to tangentially touch the outermost foil turns at each side (YMin and YMax), to generate 33 line graphs of field stress in Figures 13, 14, 15, 16, 17, and 18.

Winding	Foil Terminal Voltages (V)					
	5	4	3	2	1	0
5	1367.7	1010.8	701.0	402.2	171.3	0.0
4	1367.7	1761.3	2153.2	2555.5	2932.4	3342.9
3	5613.0	5151.1	4695.1	4232.4	3781.6	3342.9
2	5613.0	6078.3	6548.6	7010.8	7461.1	7892.9
1	10000.0	9575.3	9144.6	8730.1	8303.8	7892.9

Table 1: Voltage distribution across foil windings

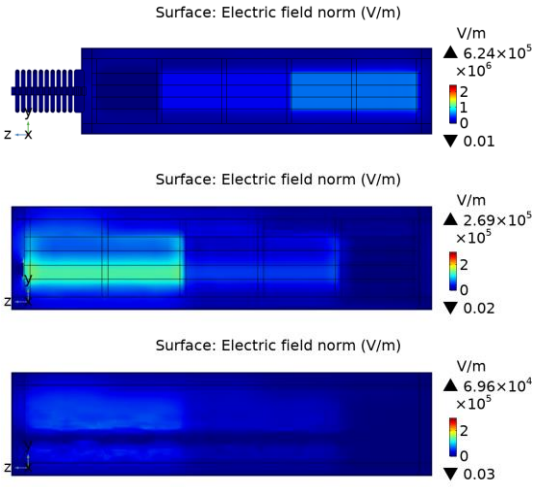

Figure 10: YZ cut planes between windings 4 and 5; winding 5 and draw lead; and draw lead and housing

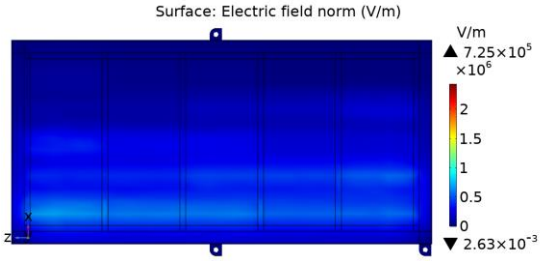

Figure 11: XZ cut plane between foils and housing

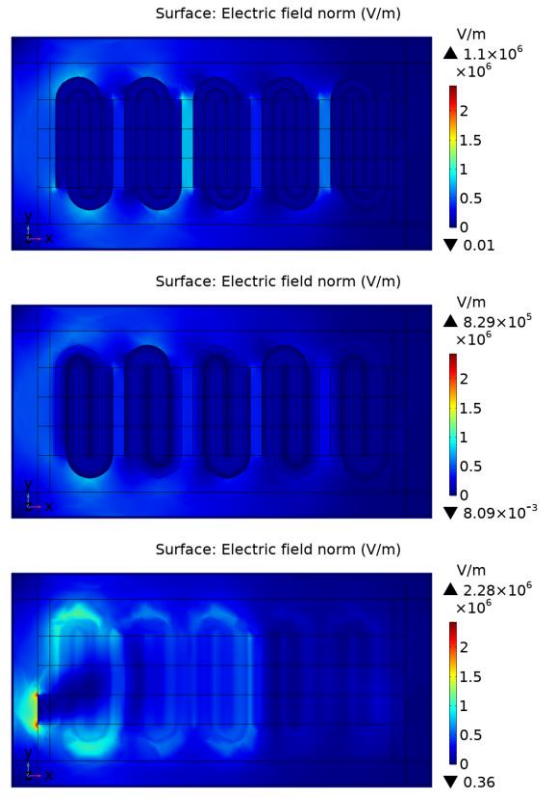

Figure 12: XY cut planes at Z2, Z2.5, and ZMax

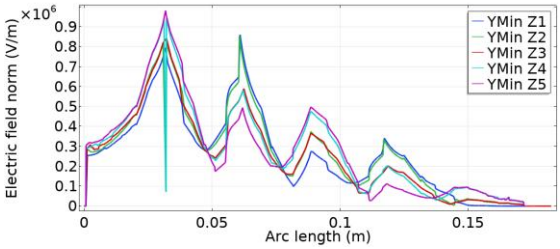

Figure 13: Field stress cut lines across elements

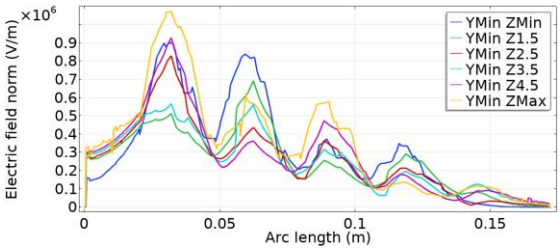

Figure 14: Field stress cut lines at ends and margins

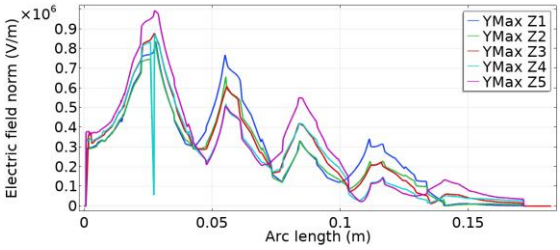

Figure 15: Field stress cut lines across elements

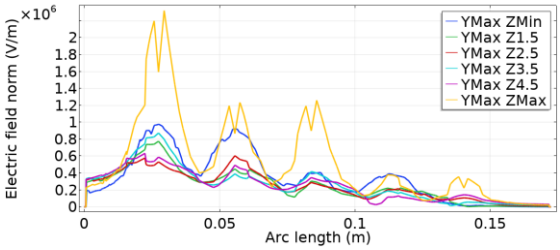

Figure 16: Field stress cut lines at ends and margins

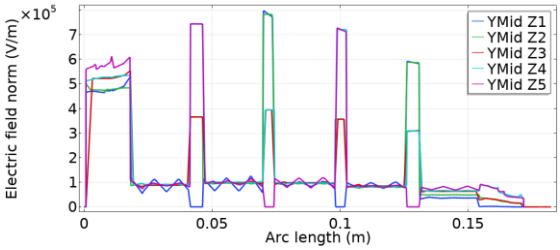

Figure 17: Field stress cut lines bisecting elements

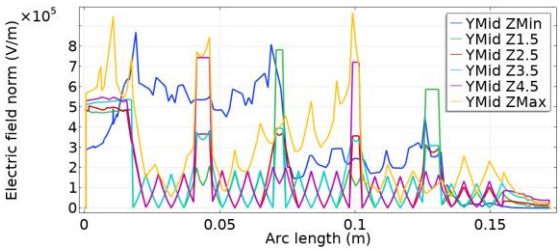

Figure 18: Field stress cut lines at ends and margins

VI. Discussion: Results

This study finds that electric field stresses are strongest where connections are made between the unit terminals and capacitive elements, and where bushings meet unit housing. This can be seen in Figure 7 and Figure 12, and these field strength maxima establish an upper bound on the normalised colour legend for diagrams in Figures 7, 11, and 12.

Table 1 and Figure 5 give an impression of the voltage distribution within the model. Between adjacent windings, stresses are strongest between neighbouring foils with greatest voltage differences and are minimised between connected foils, so the pattern of electric stresses between windings shown in Figure 7 is sensible in context of the interleaved winding arrangement when voltages are considered.

Four areas have stresses induced between adjacent foils of greatest potential difference, although Figure 7 shows that the strength of the electric field in these areas are not equal. When a nonlinear distribution of voltage is considered, it can explain the reason some of these areas experience greater stresses than others, and so the presence of nonlinear voltage distributions means that electric fields are also distributed nonlinearly within the model.

Best practice in capacitor manufacture is to fold foil edges and corners before forming each element winding. The model simulated for this study is simplistic and does not include folded corners or edges on element foils, and the sharp points which result can be seen to contribute to electrical stresses in Figures 7, 10, and 12, especially at winding ends.

Figure 11 shows a cut plane close to the tips of foil turns, and highlights field stresses which arise along the length of each winding fold. It shows that these stresses are proportionate to foil voltages, as in Figure 7, but serves also to implicate winding shape in cultivating electric field stresses. Figure 12 further supports this by showing regions of electric field stress which form around foil folds. The bend radius of folds, therefore, could affect the strength of field in these regions. If similar capacitance can be achieved using either broad or narrow element windings (large or small bend radius), from the perspective of electric field stresses the former would be preferred in any capacitor module design.

Where one foil is exposed at a dielectric margin, the electric field stresses increase around the underlying foil. This is illustrated by the middle diagram of Figure 12, and by sharper spikes in field stress values shown in Figure 18 than those in Figure 17.

The draw lead on the right of Figure 6 redirects field lines from neighbouring elements to have a distinct effect on the electric field. It thereby heightens stress on dielectric between it and the nearby winding. Since such leads must cross the entire length of the module, good design practice would have them connect to the terminal closest in voltage to the unit housing, as in the configuration used in this study. Moreover, it might be further beneficial to position the draw lead along the lower edge of the module to mitigate the effects of heat on proximal dielectrics. However, best design practise might circumvent the need for a draw lead by selecting an even number of element windings [3], such that they only need be connected at the terminal end of the capacitor unit.

Electrical field lines illustrated in Figure 6 indicate areas of increased electric field stresses within the capacitor module, highlight the presence of parasitic capacitances, and reveal fringing effects which form between elements of adjacent windings. Correspondingly, Figure 6 implies that parasitic capacitances between foil elements and housing can depend on element position: those elements in either the lowest or topmost windings appear to share a greater cross-sectional area with the module housing, which could correspond to greater coupling and therefore stronger stray capacitance effects.

The geometry used in this study is a simplistic representation of those in commercially available assets, and as such the electrical stresses between such foils could be more severe than shown here.

VII. Discussion: Methodology

In this study, electric circuit and electric currents interfaces are coupled to ascertain a voltage distribution across capacitor element foils which are: defined in the geometry as terminals in the electric currents interface; and coupled with the electric circuit interface with External U Vs. I nodes such that a voltage source can be applied. However, such nodes appear to assume that voltages refer to ground, rather than to the other terminal in the circuit (grounded or otherwise). Another approach to coupling these boundary conditions might instead allow voltages to be passed in relative rather than absolute terms, such that values can be summed rather than assumed to be with respect to ground, and would thereby allow coupling to a variety of circuit locations. By including voltmeters in the electric circuit interface which refer to the voltage at each series-connected capacitance with respect to ground, and using these voltages in an electrostatics interface, more representative electric phenomena can be illustrated for the geometrical model. Were the electric currents interface to accept relative voltages when coupled with the electric circuit interface, these interfaces could be used directly.

Configurability aids iterative development. Iteration is intrinsic to a host of development methodologies and continuous improvement principles; it is sensible for modelling to be updated as better practises and new information comes to light. Moreover, model-based techniques usually require validation in laboratory settings, and as such it is prudent to match any simulation model to the unique characteristics of a physical replica. If a model-based study can be readily updated and repeated to accommodate such characteristics, its development need not wait the prior preparation of a physical model, and the overall investigation can be streamlined. Such repetition is made easier if each step requires only minimal manual intervention.

Parameters aid such configurability. Geometry sequences can be specified based on parameters, enabling easier development of the geometry specification, allowing a model to adapt to changes specified in parameters (and thereby preparing the model for use in COMSOL's Application Builder feature), and improving readability of the geometry sequence. COMSOL's support for conditional statements in geometry sequences even allows a model's key features to adapt to user preferences, based on parameter values. Iteration is not supported, however, which makes detailed model geometries comprising many repeated components tedious and difficult to develop. Arrays offer a form of repetition but are limited in scope: the same input node can be repeated but not changed in accordance with its position. Should support for both conditional and iterative nodes be available for geometry sequences, user parameters could help establish readable, adaptable, and sophisticated model geometries which are straightforward to develop and which can scale in detail.

With support for control flow at each stage, Figure 19 shows the process steps necessary to conduct a study in COMSOL: once a geometry has been established, a comprehensive set of definitions (while not necessary) can make subsequent stages of a modelling exercise easier to configure and more resilient to changes, as materials, mesh sequencing, and boundary condition interfaces can refer to definitions specified in relation to the geometry. Good definitions are therefore key to reconfigurability and in allowing a model to adapt to change without requiring a time-intensive process

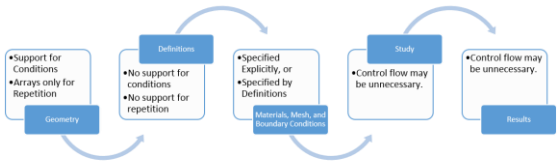

Figure 19: Stages of modelling in COMSOL

from the user to manually adjust how materials, meshes, and boundary conditions apply to an updated geometry. In contrast, explicit selections used for a mesh, materials, or boundary condition interfaces are not resilient to change and necessitate a user checking these are each correctly specified following a change to the geometry. Where a model uses parameters, definitions specified exclusively according to these parameters can adapt in line with geometrical changes, thereby reducing the manual intervention required in reconfiguring subsequent modelling stages in response to a parameter change. Thus, through definitions, a model is made much more readily changeable by adjustments required only to parameters.

However, if parameters are used for control flow through conditional or repetition declarations in a geometry sequence, but support is not provided for similar options when establishing definitions, then manual intervention is still necessary. Were COMSOL to support control flow options not only in geometry sequences, but also for definitions, users could develop models which are readily configurable by a set of parameters which apply directly to a geometry and to definitions on that geometry, and where materials, mesh sequencing, and boundary condition interfaces can be declared relative to definitions and thereby be free from the need for manual updates in response to a change in model parameters. This would allow users to create detailed and readily configurable models from a common model file, and would enrich how such models can be used in COMSOL's 'Application Builder' feature.

VIII. Conclusions

Although the model employed in this study is highly simplistic, some indicative conclusions are inferred. Field stresses are strongest around terminal connections where elements connect to the bushings, and where bushings meet the unit housing. Uneven stresses form between windings in response to voltage distributions across the elements in an interleaved, series-connected winding design, and are also affected by a nonlinear voltage distribution across capacitive elements, further contributing to their unevenness. Foil edges and sharp points give rise to stress, suggesting support for a practise of folding foils at edges and corners. Element turns contribute to field stress, which could be reduced by increased fold bend radius. Dielectric margins where winding foils interleave show increased electric field stress around the underlying foil. Finally, a draw lead cultivates stress, so designs with an even number of windings are preferred to avoid the need for one. Electric field visualisations suggest parasitic capacitances vary according to position in a unit.

Coupling between electrical circuit and electric currents interfaces assume voltages are with respect to ground, so voltmeter values are therefore first converted to an electrostatics interface to be better understood in a geometrical context. Should relative voltages be accepted between these interfaces, they could be used directly. Iterative development approaches are facilitated by model configurability, since changes are common where new information or ideas become available. Parameterisation of a model geometry can facilitate configurability, and make changes easier, particularly where parameters apply also to definitions and where those definitions form points of reference to apply materials, a mesh, and boundary condition interfaces. If control flow is supported for a geometry sequence and definitions in the form of conditional and iterative declarations (analogous to 'if' and 'loop' statements in software) then parameters can be used to influence the shape and nature of a geometry and its definitions, and therefore also the manner in which materials, mesh sequences, and boundary condition interfaces are applied. This would allow the possibility of detailed, models resilient to change, which can be made easily configurable through parameters and hence valuable to COMSOL's application builder functionality, too.

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