

A New Scheme of Symmetric Multilevel Inverter with Reduced Number of Circuit Devices

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Abstract

In this paper, a sophisticated configuration for symmetric multilevel voltage source inverters is proposed. In multilevel inverters, the costs, circuit size so installation space, complexity of control scheme and reliability are directly depended to the amount of circuit devices required. The provided comparison study among proposed inverter, CHB and recently introduced converters, validates that the proposed inverter reduces the requirements for circuit devices, including power semi-conductor switches, IGBTs, diodes, gate driver circuits and DC voltage sources. The given simulation results confirms the feasibility of the projected modular structure. Also, to approve the practicality of the proposed inverter, a prototype of the proposed topology has been implemented. Finally simulation and experimental results are compared with one another and therefore the provided comparison shows that the obtained results are in sensible agreements.

1. Introduction

With the advance of power semiconductor technology, the power electronic devices are widely used in industry to improve the manufacturing processes and system efficiency. Multilevel inverters was introduced by Nabae et al and since then, they are taken into account as an important device in power conversion process, so that they have successfully created their own way into the industry and academia as one of the popular selections of DC/AC power conversion. Multilevel inverters are basically made up of an array of power semiconductor switches, diodes and DC power supplies. Multilevel voltage source inverter (MVSI) synthesizes the input DC voltage sources to generate a stepwise output voltage. The number of output voltage waveform levels will increase as the number of input DC voltage sources increases, as well the waveform gets closer to sinusoidal. In comparison with 3 level inverters, the sinusoidal waveform of multilevel inverters can offer substantial benefits, including higher power quality, lower harmonic components, better electromagnetic interface, higher amplitude of fundamental component, higher efficiency, lower harmonic distortion, lower switching losses and lower dv/dt, that makes

multilevel inverters viable alternative for most of applications [1-8]. In the last few years much interest have been on multilevel inverters that has led to, suggestion of many new contributions and new topologies and this is still a technology under improvements. The used switching strategy in multilevel inverters will affect the quality of multilevel inverters output power, PWM and SVPWM methods are the most common approaches enabling to generate the desired output voltage waveform [9, 10]. The acceptable power quality concepts such as output voltage and current THD and so, are reported in different international standards, like IEEE-929, IEEE-1547, and EN-61000-3-2. The basic multilevel converters are assorted to 3 configurations: diode clamped (DCM), flying capacitor (FCM) and cascaded H-Bridge (CHB) multilevel inverter. Each subdivision has its own advantage and disadvantages, i.e DCM have noticeable problems with unequal current stresses and voltage unbalancing [11]. Flying capacitor multilevel inverters are less popular in industrial applications, because of their higher switching frequency that is needed to maintain the capacitor voltages balanced and also the requirement of the FC initial voltages [12]. Among various topologies of multilevel inverters, the cascaded multilevel inverters (CHB) because of their easier controllability and modularity have attracted a great deal of interest in the family of multilevel inverters. An original CHB contains number of H-bridge inverter units. Each H-bridge has a DC power supply in its input side associated with four power semi-conductor switches and can generate three levels in its output. These H-bridge units are connected in cascade or series in AC side. These inverters need least number of components compared to other two types mentioned before. Nevertheless this topology has its own disadvantages, higher number of isolated DC voltage sources and power switches are of these problems, which imposes more circuit complexity and higher total costs. Multilevel inverters can be symmetric in which the values of the DC voltage sources are equal or asymmetric in which the values of the DC voltage sources are unequal. Providing DC voltage sources with different values can be very costly making the asymmetric topologies difficult to be realized. In the symmetric multilevel inverters, the value of all DC voltage sources are equal leading to easier realization and lower design costs. However, the symmetric topologies can produce lower number of voltage levels in comparison with the

asymmetric topologies. It is noticeable that asymmetric topology increases the number of output voltage levels compared with the symmetric counterparts on the condition when both of them compose the same number of power devices. Despite the mentioned advantages of multilevel inverter, they suffer from increased number of required circuit equipment. Due to the dependence of overall costs, circuit size, reliability and control complexity on the number of DC voltage sources, semiconductor switches and related gate driver circuits of switches, the number of required circuit devices are important in multilevel inverter structures. Nowadays advanced topologies are developed to reduce the high number of components in multilevel inverters. Various cascaded based multilevel inverter with different topologies have been introduced by now. A novel MVSI, has been reported in [13]. This inverter uses bidirectional switches. Each bidirectional switch consists of two IGBTs and two diodes. If these IGBTs are connected as common emitter, then for each bidirectional switch, only one gate driver circuit is needed. The main novelty of this converter is about the reduced number of switches compared to CHB. This improvement causes a reduction on gate drive circuits. But, this topology encountered with higher peak inverse value (PIV) compared to CHB. The topology presented in [14], uses unidirectional switches. For unidirectional switches the number of gate drivers is equal to the number of switches. The number of switches and gate driver circuits are less than conventional CHB but the total PIV is more. It is known that reducing the number of switches from the conventional inverters imposes an undesired increase in total PIV value. With proper connection of power switches to DC voltage sources, this increase can be limited. Comparatively, the PIV of [14] is reduced considerably to that of [13]. Also it must be mentioned that, since the number of IGBTs, switches and gate driver circuits are reduced significantly, an increase in total PIV is acceptable and can be neglected while this increase cannot detract from its values of obtained benefits from reductions. Recently, a novel MVSI has been suggested, that is reduced the power components [15] compared to CHB. Moreover, this inverter has kept the PIV equal to CHB.

The main contribution of this paper is proposing an advanced configuration for the symmetric multilevel voltage source inverter. This topology is inspired of the idea behind conventional CHB. This inverter reduces the requirements for circuit devices compared to conventional CHB and the recently proposed CHB based inverters in [13-15]. In this regards, the proposed inverter is analyzed and then a full comparison is provided to validate the superiority of the proposed multilevel inverter. The lower number of requirements for circuit devices results lower costs and the installation area, higher reliability and ease of implementation and simpler control scheme. The remainder of this paper is organized as follows: the structure and details of proposed topology are described item by item in section 2. A full comparison between the suggested inverter and the well-known inverters is represented in section 3. Both simulation and experimental outcomes are given in section 4. Finally, section 5 represents the conclusion.

2. Proposed Configuration

Fig. 1(a) shows the basic cell of the proposed multilevel structure. As seen in this figure, the basic unit consists of five semiconductor unidirectional switches and three insulated DC

voltage sources. The proposed cell is symmetric, so, the values of DC sources are equal. Each unidirectional switch includes an IGBT and an anti-parallel fast recovery diode. Each basic unit can generate four levels in its output, contains three positive steps and one zero value. Table 1 indicates switching states of the basic unit of the proposed structure for each output voltage value. In the proposed unit, the related switches must be controlled in order to avoid short circuit. Thus, in this Table, 1 and 0 indicate the on and off states of the switches, respectively. The tantamount circuits for different output voltages of basic unit of the symmetric MVSI are shown in Fig 1 (b)-(d).

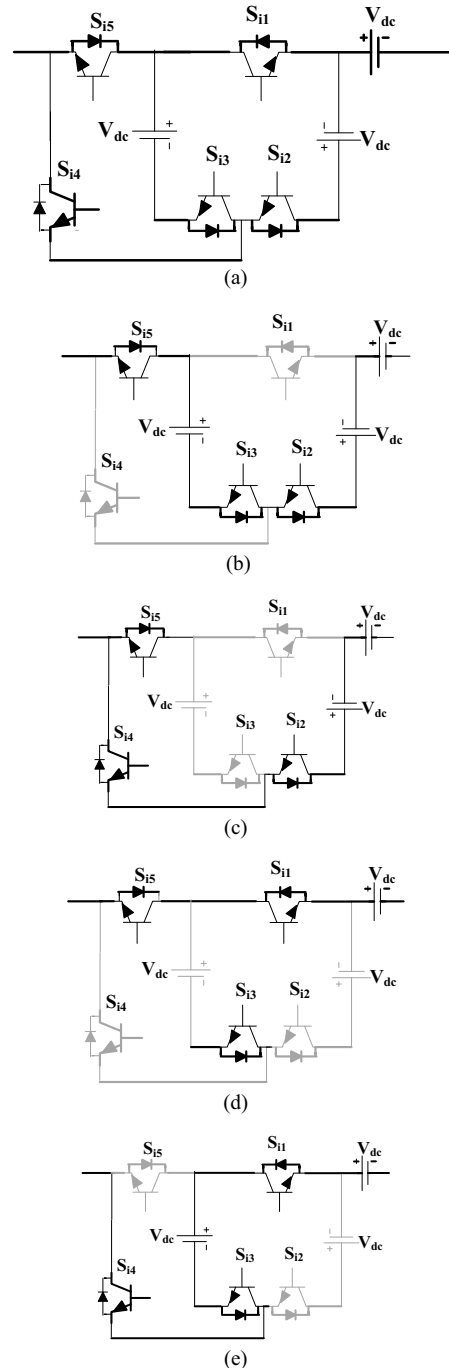


Fig. 1. a) Circuit diagrams of the proposed MVSI basic cell and equivalent circuits for; b) $3V_{dc}$, c) $2V_{dc}$, d) V_{dc} , and e) zero level.

Table 1. Various switching states of i -th suggested basic cell

State	S_{i1}	S_{i2}	S_{i3}	S_{i4}	S_{i5}	V_o
1	0	1	1	0	1	$+3V_{dc}$
2	0	1	0	1	1	$+2V_{dc}$
3	1	0	1	0	1	$+V_{dc}$
4	1	0	1	1	0	0

The generalized view of the proposed MVSI is represented in Fig. 2. As shown, the proposed structure contains of series connection of k -basic units, two DC sources, associated with six semiconductor unidirectional switches. The switches of H_U, H'_U, M, M', H_L and H'_L are well configured, so that the proposed inverter can generate all the possible voltage steps with the value of positive and negative in the output. The mentioned independent DC voltage sources are pointed by V_{dc} and V_s .

The amplitude of V_s that is series with the basic units is set pursuant to the number of required DC voltage sources. And the number of DC sources is depended to the number of output voltage levels. In this regards, V_s can be either zero or any values of V_{dc} or $2V_{dc}$. As illustrated in this figure, the proposed topology is composed by n -isolated DC voltage sources. Rectifiers connected to isolated transformers fed from AC voltage can produce different DC voltage sources [16]. Also, the required DC voltage sources in this structure can be achieved by applying renewable energy sources such as photovoltaic cells or fuel cells, or with energy storage devices, like batteries. It is notable that the proposed MVSI is symmetric, so the required DC voltage links must be equal in values. The quality of the output voltage may be deteriorated due to the inequality of DC voltage sources and as a result of inequality of voltage levels. In this regards, undesired harmonics can be generated in the output voltage. In whatever way, the notable point is that producing balanced DC voltage sources is the same problem among all symmetric inverters. In some cases, supplementary circuits, to provide equal DC voltages, are required for symmetric inverters. For instance, if the PV panels are employed as DC voltage sources, they have already equipped with DC/DC converters for voltage level adjustments. The DC voltage sources can be produced by using transformers and rectifiers. Nevertheless, the undesired changes in the DC voltage sources can be compensated by complementary modulation strategies [17, 18]. The implementation of these methods needs the manipulation of the inverters hardware by additional devices and circuits, and makes the control scheme more intricate. As the proposing a novel structure for multilevel inverters is the main goal of this paper, so countervailing differences of DC voltages which can be done by modulation methods, is not taken into consideration. A provided output phase voltage is the sum of individual voltages of DC power supplies amplitudes. So, the maximum obtainable value for the output voltage ($V_{o,max}$) of the introduced MVSI can be calculated by the following equation:

$$V_{o,max} = \sum_{i=1}^n V_i \quad (1)$$

where n -is the number of DC sources. The number of output voltage levels (m) can be obtained using the following equation:

$$m = 2 \frac{V_{o,max}}{V_{dc}} + 1 \quad (2)$$

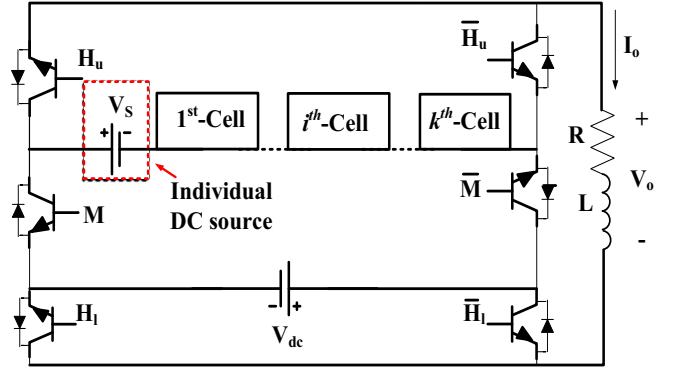


Fig. 2. Proposed MVSI

The proposed cascaded multilevel inverter is as symmetric inverter. So, increasing the number of cells is the solution to reach a definite value in the numbers of output voltage levels. In order to clarify the proposed inverter's characteristics, it is needed to specify the parameter L . L is an integer number and $L = 1, 2, 3, \dots$. It is obvious that to generate m -levels in the output voltage, n -DC sources are needed. That is:

$$n = \begin{cases} \frac{m-1}{2}; & \text{if } m = 6L + 3 \\ \frac{m-1}{2}; & \text{if } m = 6L + 5 \\ \frac{m-1}{2} - 1; & \text{if } m = 6L + 7 \end{cases} \quad (3)$$

Since each cell consists of three DC voltage sources, so with n DC links, it is possible to have k basic cells. It is clear that, in this configuration n must be in a proper relationship with k . So:

$$k = \begin{cases} \frac{n-1}{3}; & \text{if } m = 6L + 3 \\ \frac{n-2}{3}; & \text{otherwise} \end{cases} \quad (4)$$

As said before, the value of V_s is set according to the number of output voltage levels. In the following the relationship between V_s and m is mathematically formulated:

$$V_s = \begin{cases} 0 & \text{if } m = 6L + 3 \\ V_{dc} & \text{if } m = 6L + 5 \\ 2V_{dc} & \text{if } m = 6L + 7 \end{cases} \quad (5)$$

For simplicity, when it is required to generate m -levels in output voltage, the number of required DC sources must be obtained using (3) and the value of V_s must be chosen according to the given formula in (5). For instance to generate 9-levels in output voltage, the number of DC links is four and then V_s is set to be zero. Also, for $m = 11$ and 13 the number of DC voltage sources is calculated to be five. And then V_s is obtained to

be $V_s = V_{dc}$ and $2V_{dc}$, respectively. In the suggested inverter, the number of switches (N_{switch}) is calculated by (6):

$$N_{Switch} = \begin{cases} \frac{5n+13}{3}; & \text{if } m = 6L+3 \\ \frac{5n+8}{3}; & \text{otherwise} \end{cases} \quad (6)$$

Moreover, the equation between the number of output levels (m) and the number of switches (N_{switch}) is as follows:

$$N_{Switch} = \begin{cases} \frac{5m+21}{6}; & \text{if } m = 6L+3 \\ \frac{5m+11}{6}; & \text{if } m = 6L+5 \\ \frac{5m+1}{6}; & \text{if } m = 6L+7 \end{cases} \quad (7)$$

Each switch requires a separate driver circuit to produce switching pulses, thus the number of driver circuits is equal to the number of power switches, too. So:

$$N_{Driver} = N_{Switch} \quad (8)$$

The total peak inverse voltage PIV of switches is the other essential parameter of the inverter which is calculated as follow:

$$PIV = \sum_{j=1}^{N_{Switch}} PIV_{Switch_j} \quad (9)$$

So, the below formulations are used to calculate the total PIV :

$$PIV^{p.u.} = \begin{cases} \frac{19n-7}{3} - \frac{7}{3}; & \text{if } m = 6L+3 \\ \frac{19n-14}{3} - \frac{14}{3}; & \text{if } m = 6L+5 \\ \frac{19n-2}{3} - \frac{2}{3}; & \text{if } m = 6L+7 \end{cases} \quad (10)$$

In symmetric mode, the relationships between PIV and m is formulated as follows:

$$PIV^{p.u.} = \begin{cases} \frac{19m-33}{6}; & \text{if } m = 6L+3 \\ \frac{19m-47}{6}; & \text{if } m = 6L+5 \\ \frac{19m-61}{6}; & \text{if } m = 6L+7 \end{cases} \quad (11)$$

3. Comparison of the Proposed Inverter with Other Multilevel Inverters

Generating the specific number of output voltage levels by using less number of circuit devices is the main goal of introducing the proposed symmetric structure. The purpose of this section is to compare the major parameters such as IGBTs, gate driver circuits, DC voltage sources and total PIV among the proposed multilevel inverter and the conventional symmetric MVSIs reported in literatures. Comparing the proposed inverter with symmetrical inverters is fair and rational. It is pointed out that the proposed inverter is indicated by **P** and the other symmetric inverters participated in comparison study are shown by **R₁**–**R₄** in these comparisons. The conventional symmetric cascaded H-bridge inverter is referred to as **R₁**. The proposed system of [15] is **R₂**, while **R₃** is related to [13]. Finally, the system in [14] is referred to as **R₄**. The comparison of MVSIs is discussed versus output voltage levels. In this regards, it is assumed that the maximum output voltage is equal for all mentioned inverters. The numbers of IGBTs versus the number of voltage levels for various MVSIs configurations are

represented in Fig. 4. The proposed inverter uses unidirectional switches, then the number of gate drivers is equal to N_{switch} . However, **R₃**, has several bidirectional switches in its topology. Each bidirectional switch consists of two IGBTs. Since these IGBTs are connected as common emitter, then for each bidirectional switch, only one gate driver circuit is needed. Assuming this concept, the number of gate driver circuits versus output voltage levels are shown in Fig. 5.

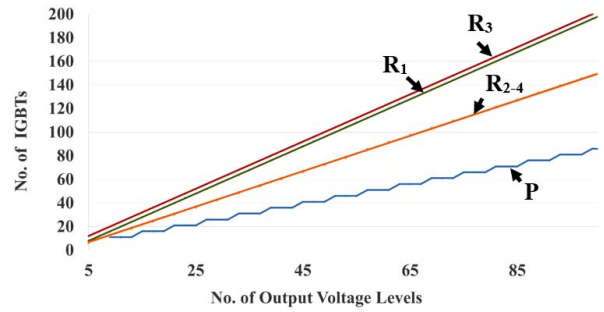


Fig. 3. Number of IGBTs versus number of levels for proposed topology and other mentioned solutions

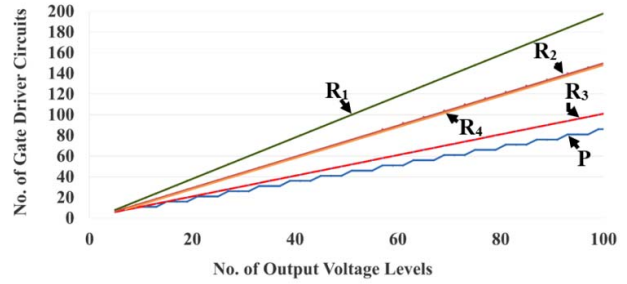


Fig. 4. Number of gate driver circuits versus number of levels for proposed topology and other mentioned solutions

Regarding Figs. 3&4, in the all range of possible voltage levels, the proposed topology reduces the requirements for IGBTs and gate driver circuits in comparison with other mentioned solutions. Therefore, less components result in reduction in the required installation area and the costs. Also, the control scheme gets simpler and the reliability of overall system is enhanced as well. The number of required DC voltage sources is another parameter plays a key role on overall inverter costs. Fig. 5 shows the number of DC voltage sources versus output levels in all mentioned inverters.

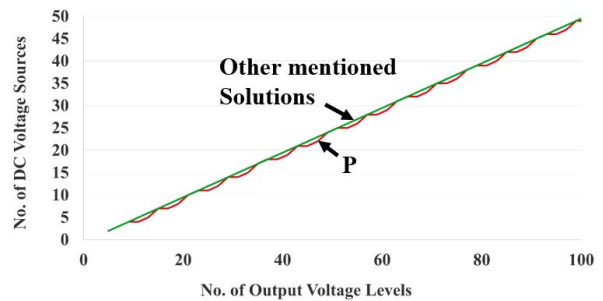


Fig. 5. The number of DC voltage sources versus number of levels for proposed topology and other mentioned solutions

By considering the above Figs., it can be understood that in order to achieve the same level in the output, the number of required DC voltage sources in the proposed symmetric inverter is mostly keeps close to other presented structures and in some output levels is lower. Another essential parameter which plays a consequential role on overall inverter expense is the voltage ratings of power switches. It is known that reducing the number of switches from the conventional inverters imposes an undesired increase in total *PIV* value. With proper connection of power switches to DC voltage sources, this increase can be limited. Fig. 6 depicts the value of considered inverters.

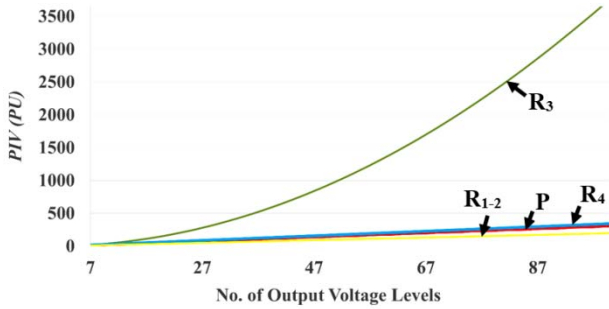


Fig. 6. Total *PIV* value versus number of levels for proposed topology and other mentioned solutions

Because of the big reduction in circuit equipment in the proposed inverter, a bit increase in its total *PIV* compared to some conventional inverters is acceptable and can be neglected, while a reduction in number of switches, gate driver circuits and DC power supplies are achieved.

4. Simulation and Experimental Results

In order to verify the correct performance of the proposed multilevel inverter in generating all output voltage levels, the both simulation and experimental results have been provided. The converter is simulated by MATLAB/Simulink software. Then, to validate the practicability and the good performance of the suggested MVSI, experimental results are obtained and compared with those of simulation ones. To provide the DC voltage links, the adjustable DC sources existing in the laboratory, have been used. Table 2 represents the main parameters of implemented circuit.

Table 2. Parameters of the implemented inverter.

Type of switch	IRF260
Type of MOSFET driver	Hcpl316j
Pulse Generator	AVR mega 32
DC Voltage Sources Magnitudes	$V_{dc} = 30V$
Series R-L Load Parameters	30 Ohm & 20mH
Fundamental Frequency	50Hz

Different switching strategies are introduced to improve the quality of output voltage waveform. For instance, fundamental frequency-switching, sinusoidal PWM, selective harmonic elimination (SHE-PWM), space vector PWM (SV-PWM), and others are such the modulation techniques that apply for this

purpose. The fundamental frequency-switching scheme is applied in this study because of low switching frequency of it [19]. For power converters, the total harmonic distortion (*THD*) is an important indicator that evaluates the quantity of harmonic contents in the output waveform. The *THD* is defined as follows: The ratio of the sum of the RMS value of power of all harmonic components to the RMS value of power of the fundamental frequency component is defined as *THD*. So the following equation gives the *THD* value.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_{o_n}^2}}{V_{o_1}} = \sqrt{\left[\frac{V_{o_{rms}}}{V_{o_1}}\right]^2 - 1} \quad (12)$$

In this equation, n -represents the order of the corresponding harmonic, while the sub-index 1 corresponds to the fundamental frequency. Hence, V_{o_n} and V_{o_1} are the rms of the n order harmonic and fundamental of the output voltage, respectively. Also, $V_{o_{rms}}$ represents the rms magnitudes of the output voltage.

In above relation, the value of V_{o_1} and $V_{o_{rms}}$ can be obtained using the following equations, respectively:

$$V_{o_{rms}} = \frac{2\sqrt{2}}{\pi} V_{dc} \sqrt{\sum_{m=1,3,5,\dots}^{\infty} \left(\sum_{j=1}^{N_{Level}} \frac{\cos(m\theta_j)}{m} \right)^2} \quad (13)$$

$$V_{o_1} = \sum_{j=1}^{N_{Level}} \frac{2\sqrt{2}}{\pi} V_{dc} \cos(\theta_j) \quad (14)$$

Where, the values of $\theta_1, \theta_2, \dots, \theta_{N_{Level}}$ represent switching angles and is calculated by:

$$\theta_j = \sin^{-1}\left(\frac{j-0.5}{N_{Level}}\right) \quad j=1,2,3,\dots,N_{Level} \quad (15)$$

It is clear that the value of *THD* depends on the number of levels and so, switching angles. It is important to mention that removing the selective harmonics and reducing the total harmonic distortion are not the goal of the presented paper. And this switching scheme is only used to generate the desired voltage steps. Fig. 7 shows the circuit diagram of the 11-Level multilevel inverter.

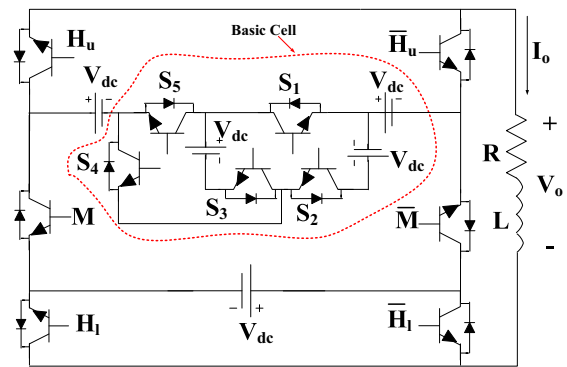


Fig. 7. Circuit diagram of 11-Level multilevel inverter

Table 3 illustrates the switching states of the symmetric 11-level suggested inverter.

Table 3. Switching states of proposed symmetric 11-level inverter

Output Voltage	H _l	M	S ₁	S ₂	S ₃	S ₄	S ₅	H _u
$5V_{dc}$			0	1	1	1	1	0
$4V_{dc}$			1	1	1	1	1	0
$3V_{dc}$			0	1	0	--	0	
$2V_{dc}$			1	1	0	--	0	
V_{dc}			0	1	--	--	1	
0			0	0	--	0	1	--
$-V_{dc}$			1	0	--	--	0	
$-2V_{dc}$			0	0	1	--	1	
$-3V_{dc}$			1	0	1	--	1	
$-4V_{dc}$			0	0	0	0	0	1
$-5V_{dc}$			1	0	0	0	0	1

The voltage and current waveform of the simulated 11-level proposed inverter are shown in Fig. 8.

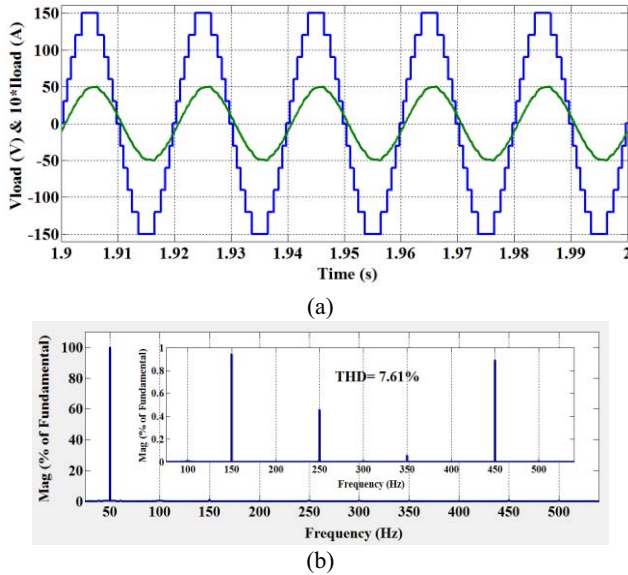


Fig. 8. a) Voltage and current waveforms and b) harmonics content of voltage of the proposed 11-level inverter

As it can be seen, all the voltage levels can be generated in the suggested inverter which validates the practicability of proposed inverter. To confirm the feasibility of the suggested multilevel inverter, the measured output voltage and current waveforms of implemented single phase prototype of the 11-level proposed inverter are shown in Fig. 9 (a) and (b).

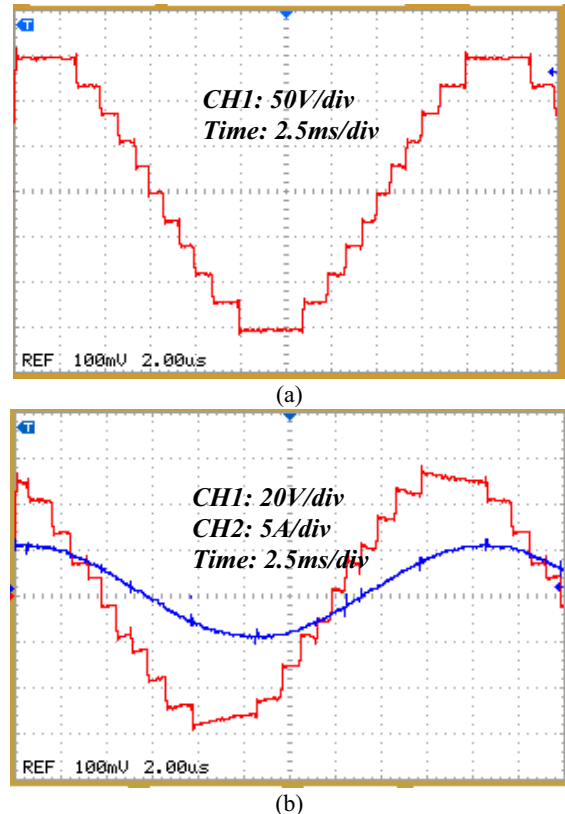


Fig. 9. Experimental results of implemented 11-level proposed inverter. a) Output voltage (no load), b) output voltage and current.

The provided results confirm that the proposed inverter is able to generate the desired output voltage waveform. These figures show good agreements in the simulation and experimental results. The negligible difference between the magnitudes of the simulation and experimental results is due to voltage drops on switches in the prototype.

5. Conclusions

The main purpose of this paper is to propose an advanced structure for symmetric multilevel voltage source inverters. This novel modular configuration applies reduced number of circuit devices, such as its power switches, diodes, IGBTs, gate driver circuits of switches and DC voltage sources. The lower number of needed circuit equipment results remarkable reduction in general costs and installation area, improved reliability and simpler control procedure.

In order to demonstrate the performance of the proposed inverter over the conventional CHB and recently proposed symmetric inverters a full comparison study is provided. Also, a prototype of the proposed topology has been implemented to validate the practicability of the recommended structure. At the end of the paper, the provided simulation and experimental results are compared with each other to demonstrate the good compromise of the achieved results.

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